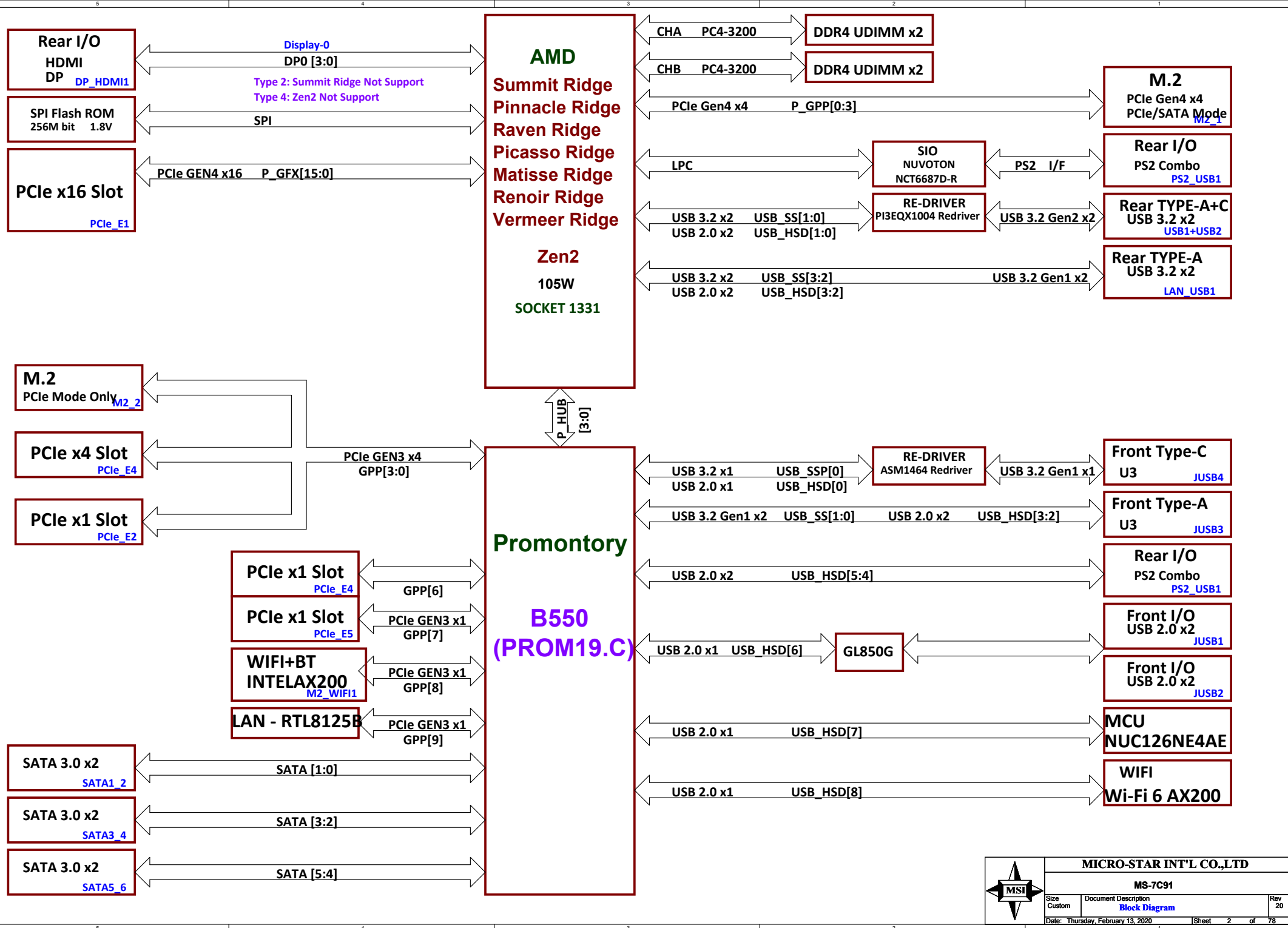
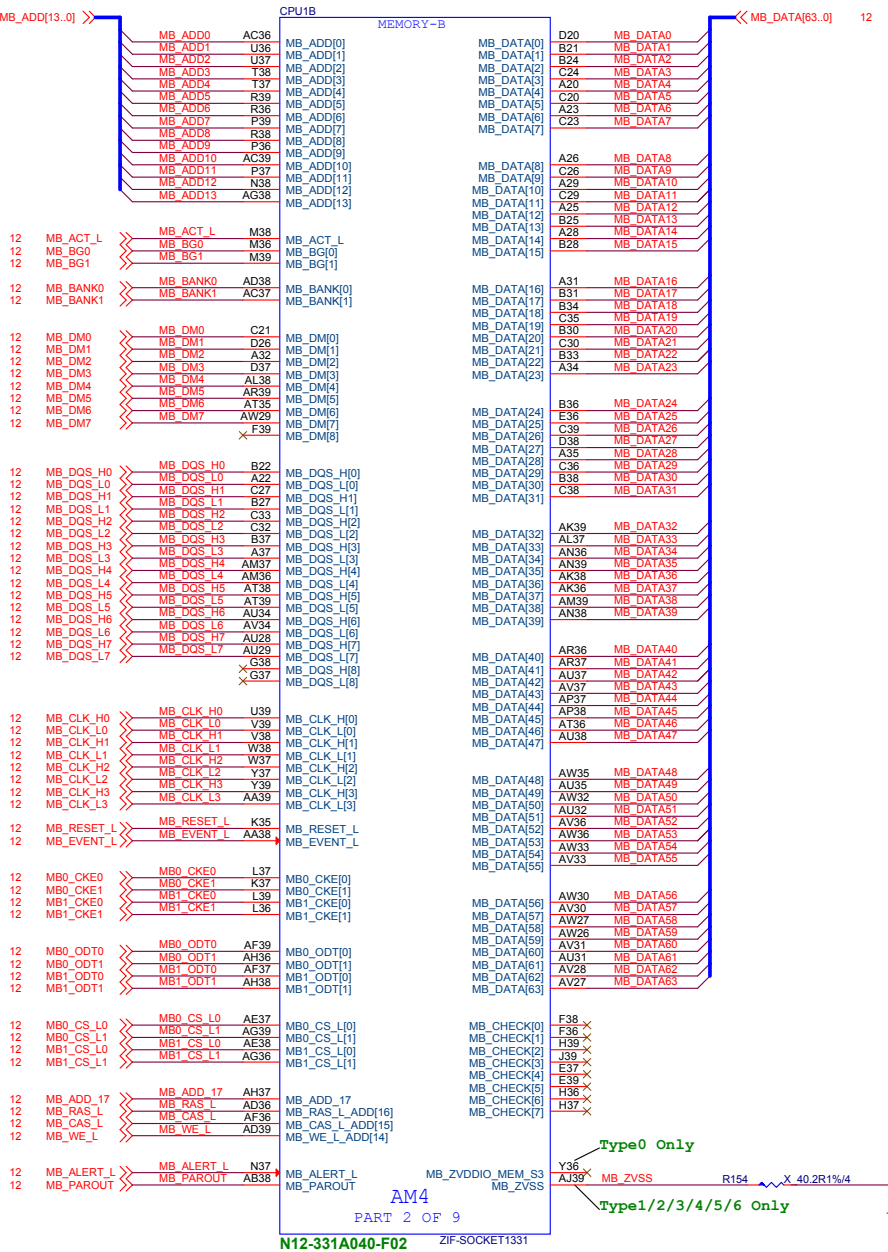
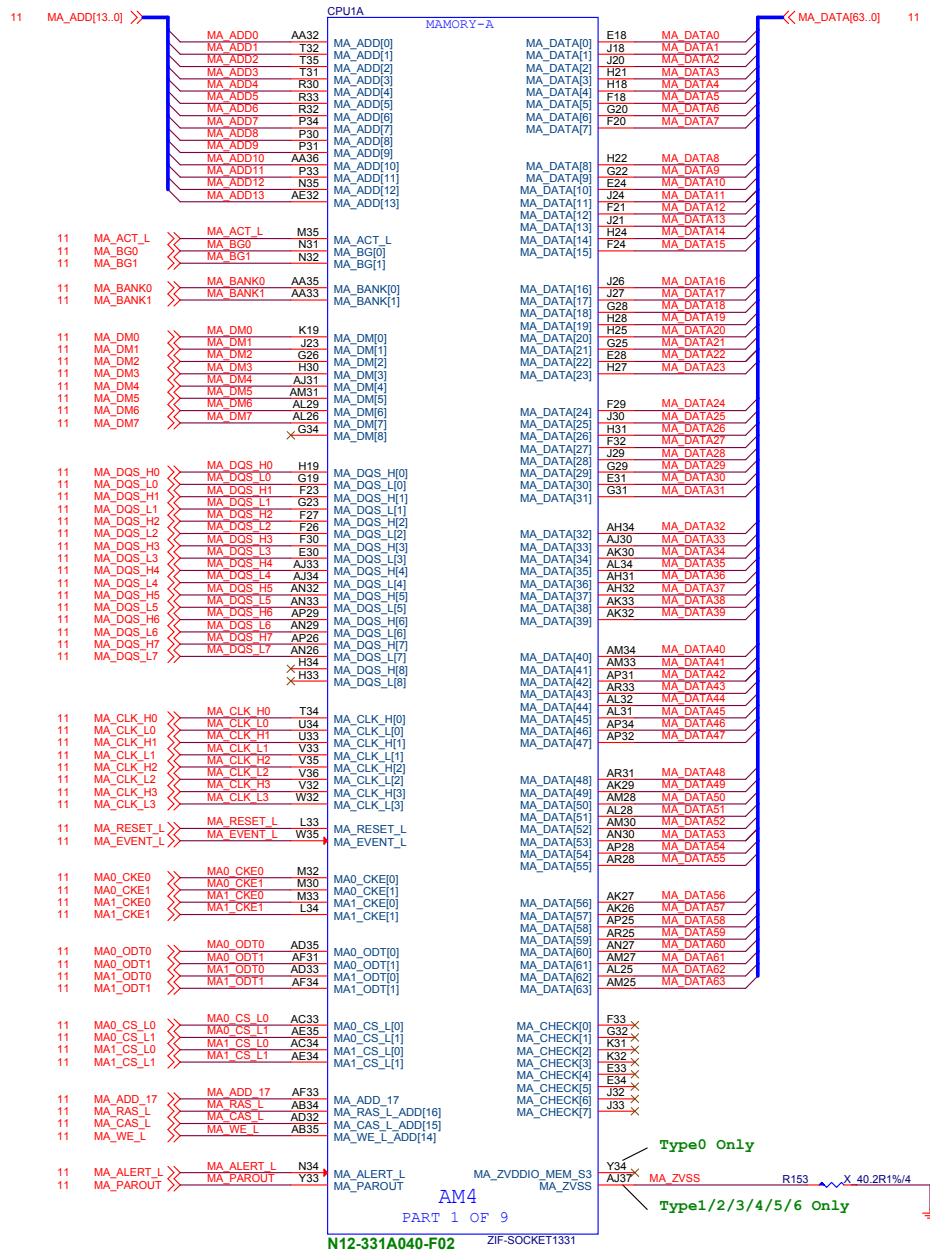


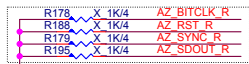
# AMD AM4 B550

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34	LAN - RTL8111H	65	ATX Power - FrpntPanel / EMI		
35	LAN - RT8125B	66	LED - EZDEBUG / AMP		

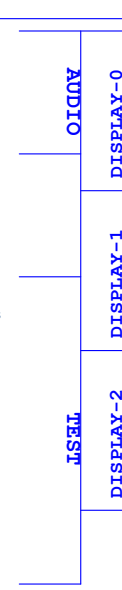
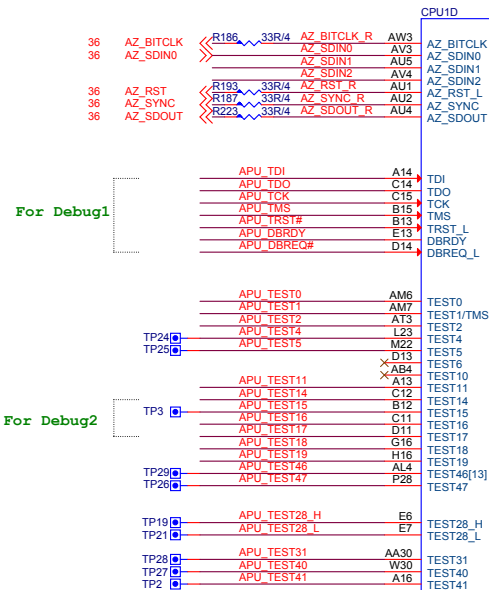
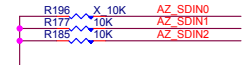
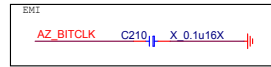








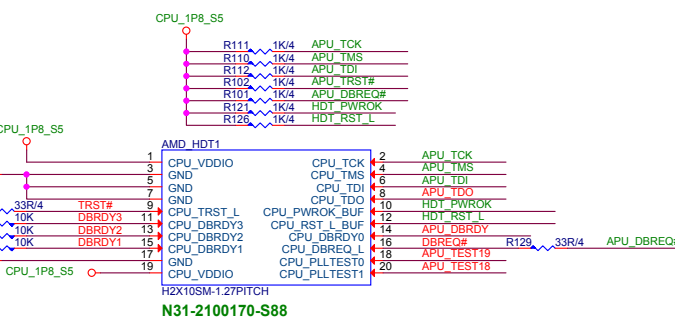
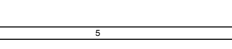
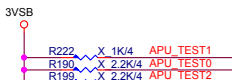
Type0 Only



For HDMI

For DP

Not supported on TYPE 2/4



N31-2100170-S88

N12-331A040-F02

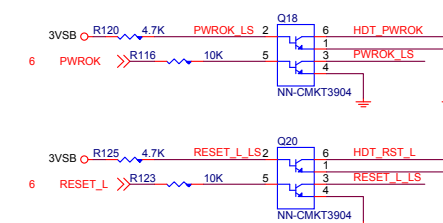
ZIF-SOCKET1331

AM4  
PART 4 OF 9

K14 PIN: 有HDMI SPEC的話需Pull-up  
ENBLE功能

For Debug2

Not support Type2

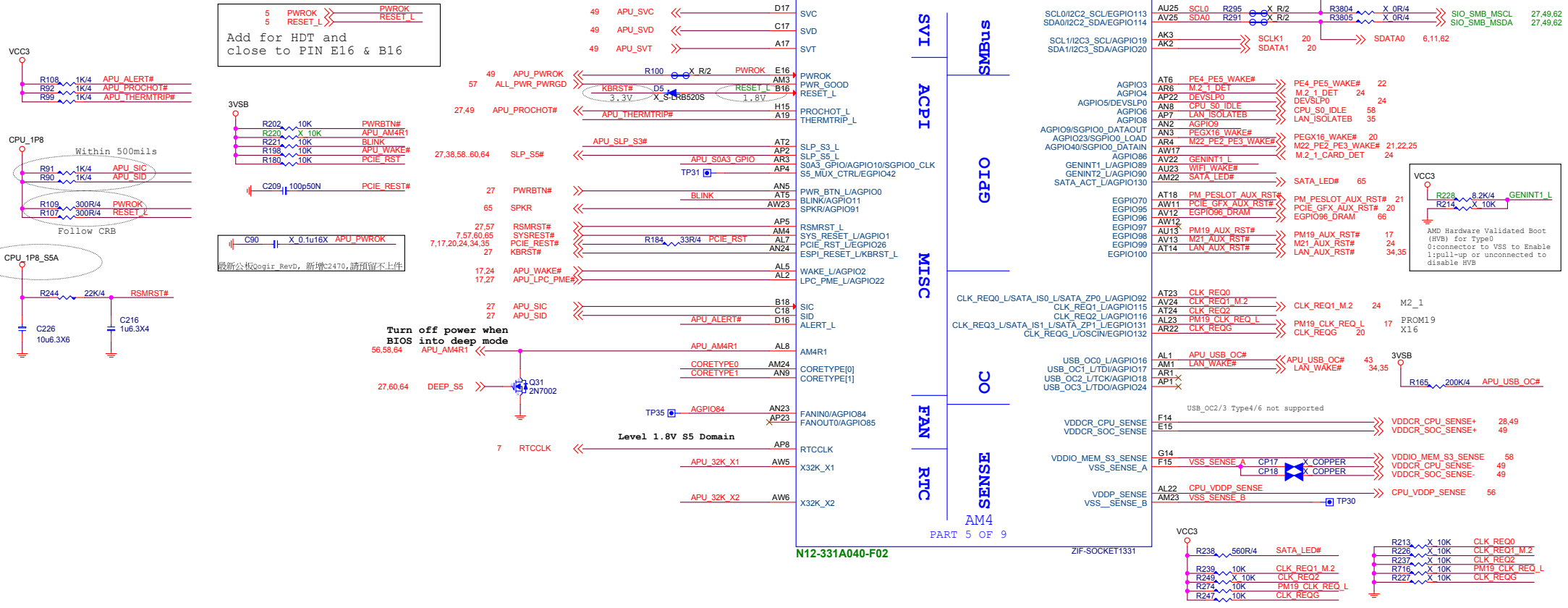


**MICRO-STAR INT'L CO.,LTD**

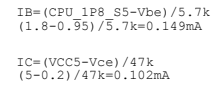
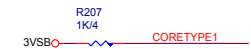
**MS-7C91**

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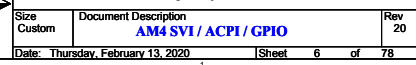


Layout: Place x'tal within 1.5 inch of APU



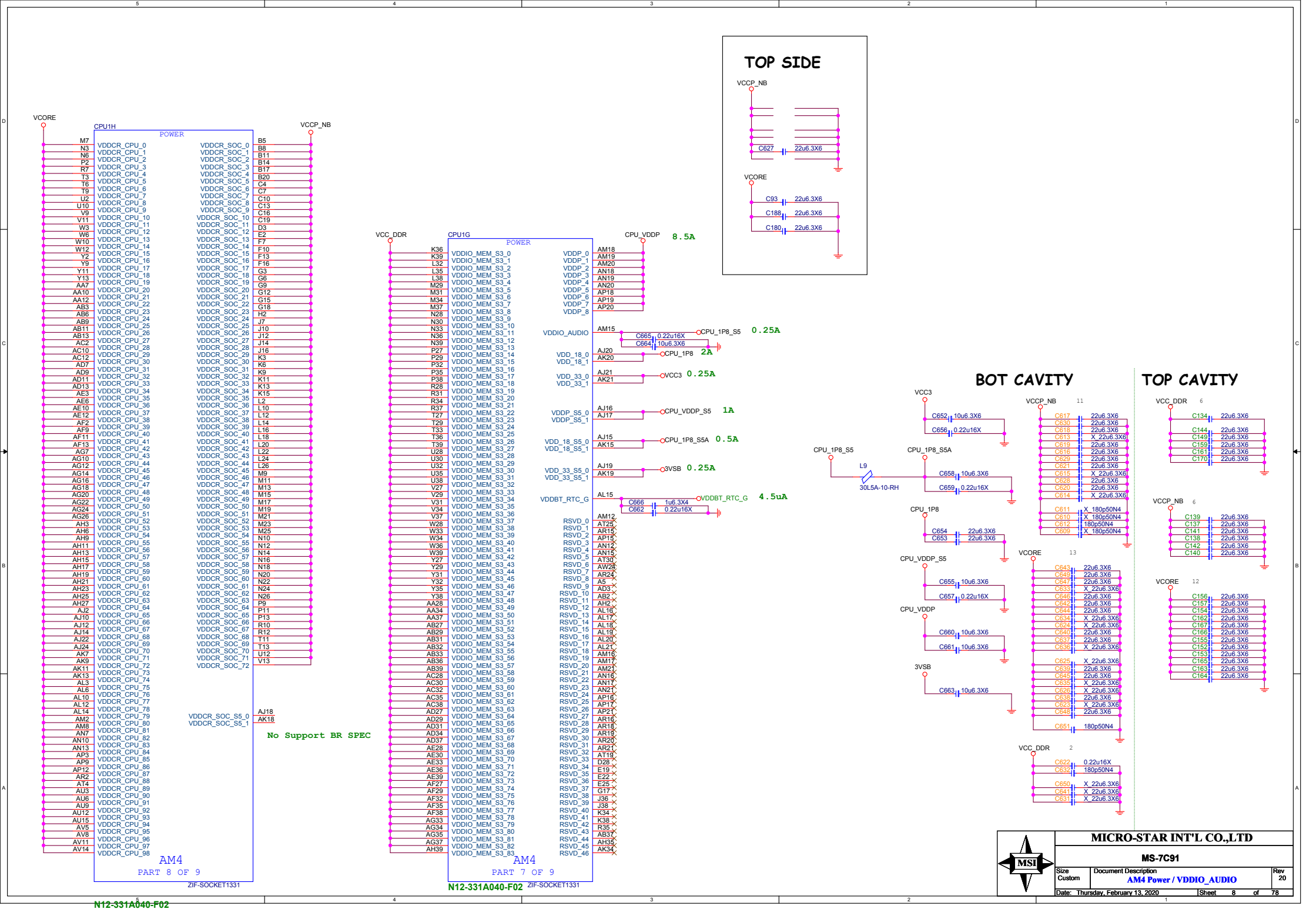
**SPEC no Support**

The schematic shows the SPI TPM\_HOLD# signal. It is a pull-up circuit with two sources: 3VSB (via R171, 10K) and PWR\_1P8\_SW (via R262, 10K). The signal is connected to the AGPIO9 pin and the SPI\_TPM\_HOLD# pin.

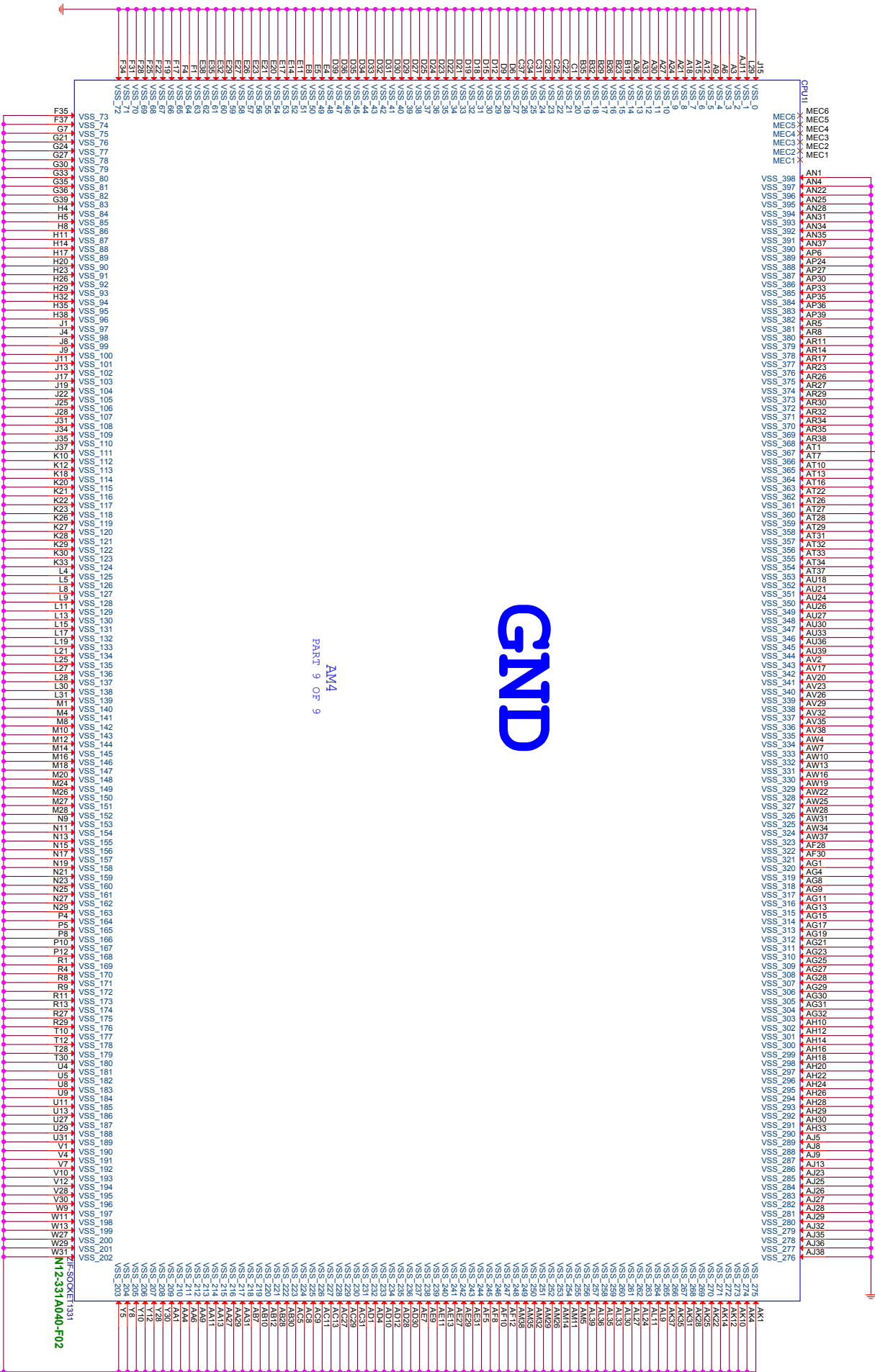
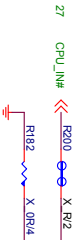




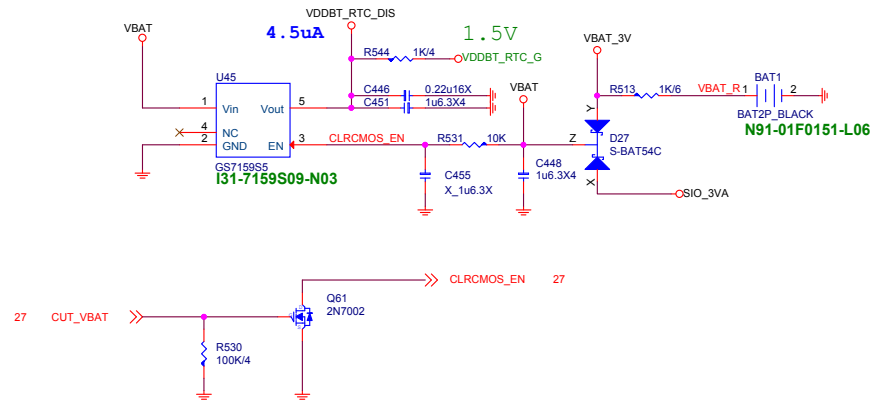




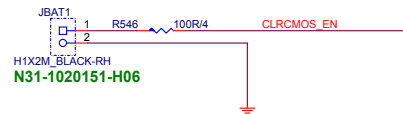




## RTC & Clear CMOS Circuit



### Clear CMOS button



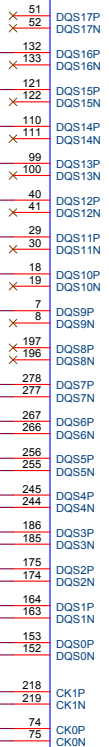
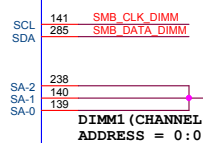
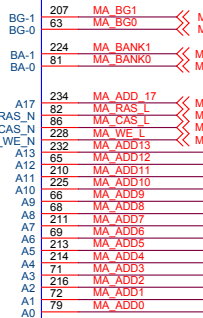
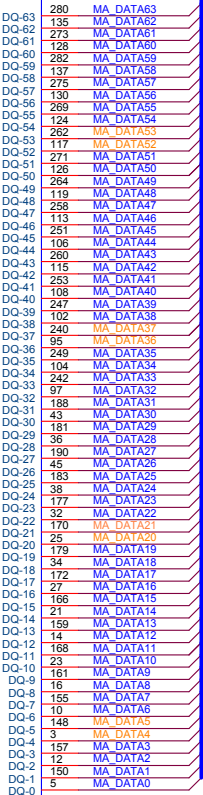
**MICRO-STAR INT'L CO.,LTD**

MS-7C91

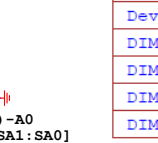
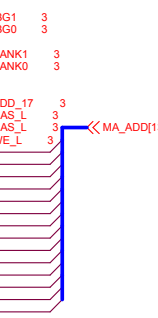
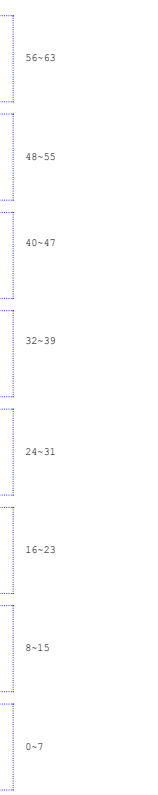
Size Custom	Document Description <b>RTC / CMOS</b>	Rev 20
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A1 A2 B1 B2

DIMMA1A

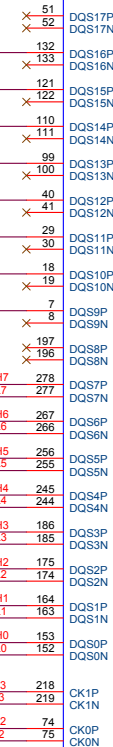
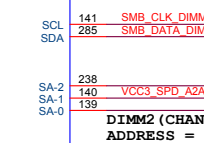
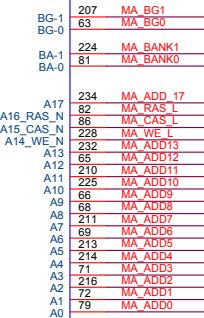
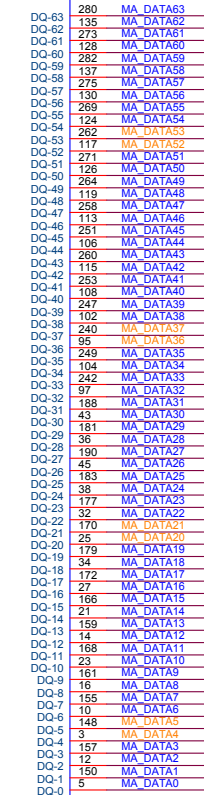
DDRIV-288P\_BLACK  
N13-2881281-L06DIMM1 (CHANNEL-A) -A0  
ADDRESS = 0:0 [SA1:SA0]

&lt;&lt; MA\_DATA[63..0] 3..11

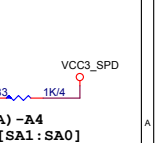
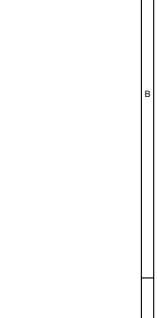
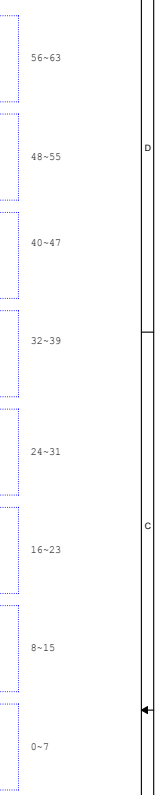
DIMM1 (CHANNEL-A) -A0  
ADDRESS = 0:0 [SA1:SA0]


SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

DIMMA2A

DDRIV-288P\_BLACK  
N13-2881281-L06DIMM2 (CHANNEL-A) -A4  
ADDRESS = 1:0 [SA1:SA0]

&lt;&lt; MA\_DATA[63..0] 3..11

DIMM2 (CHANNEL-A) -A4  
ADDRESS = 1:0 [SA1:SA0]



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Size Custom Document Description

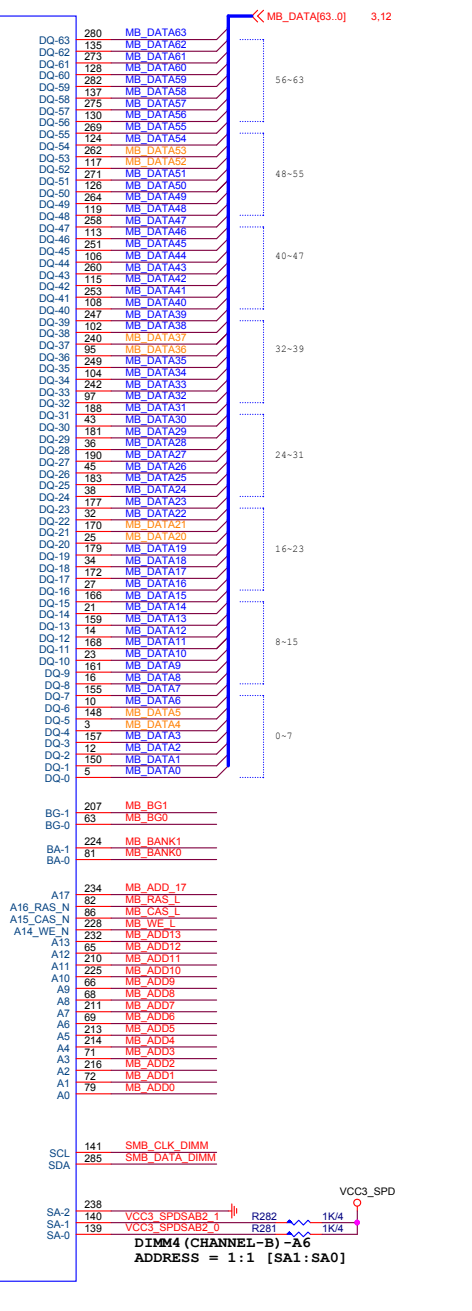
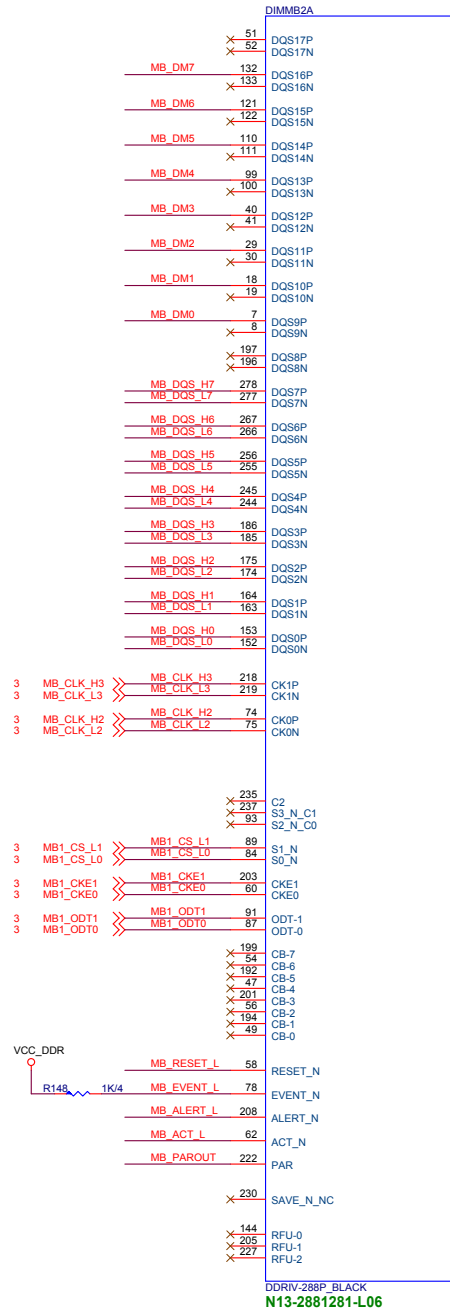
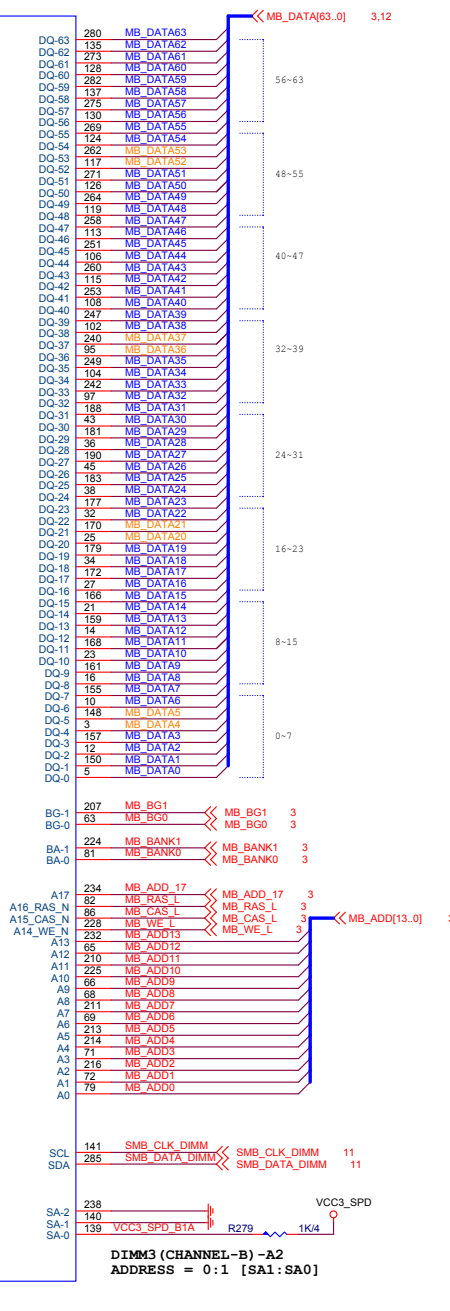
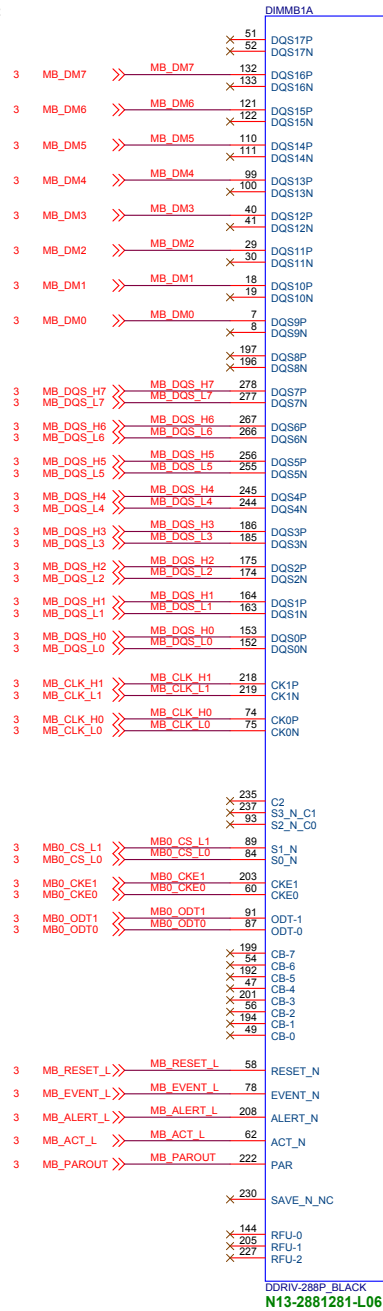
DDR4 - DIMM CH-A

Date: Thursday, February 13, 2020

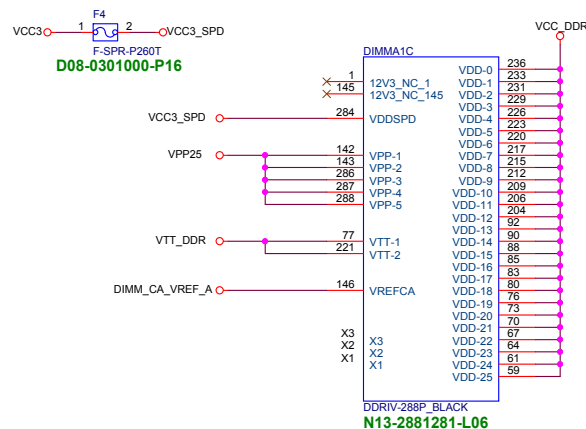
Sheet 11 of 78

Rev 20

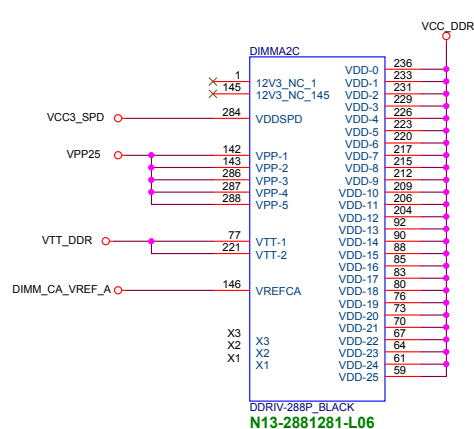
6.62 SCLK0 >>> SCLK0 R294 X R/2 SMB\_CLK\_DIMM >>> SMB\_CLK\_DIMM 12  
6.62 SDATA0 >>> SDATA0 R290 X R/2 SMB\_DATA\_DIMM >>> SMB\_DATA\_DIMM 12



av1:D08-0301100-B07

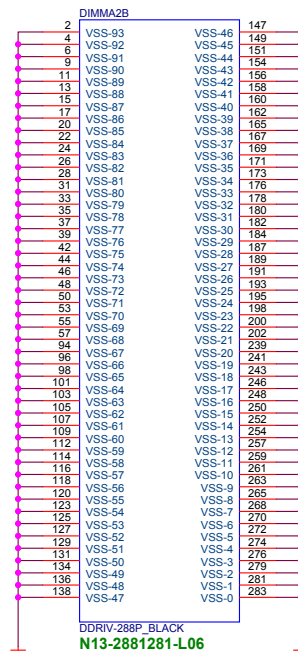
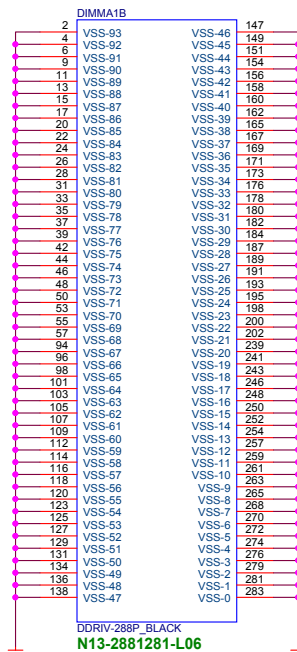
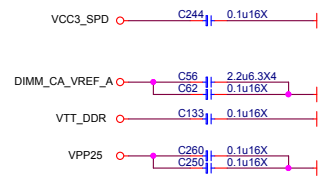
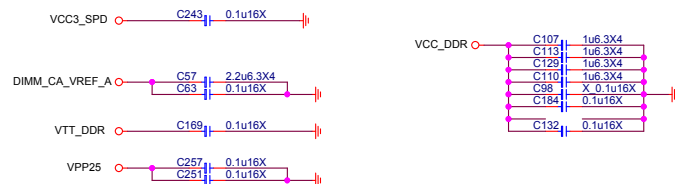
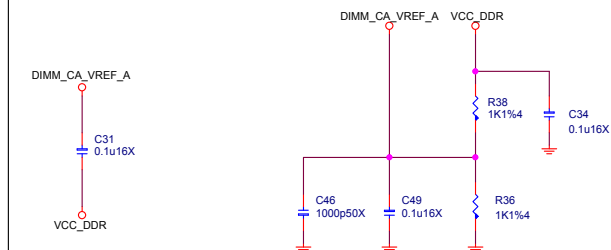


DIMM SLOT PN BY SPEC



## DDR VREF

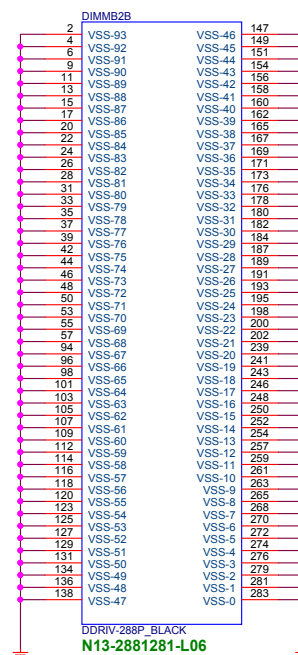
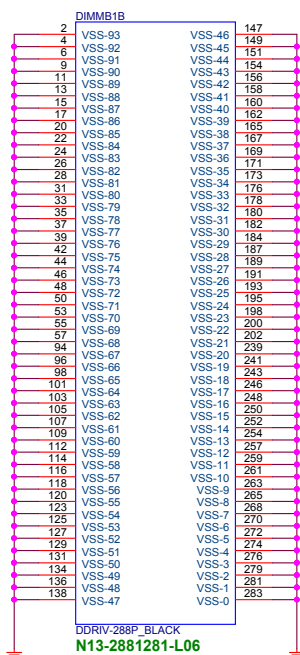
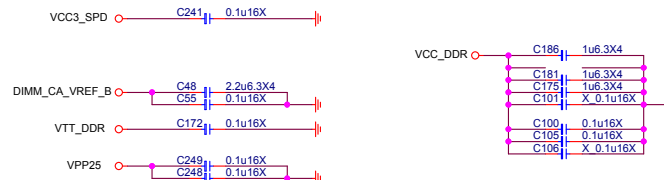
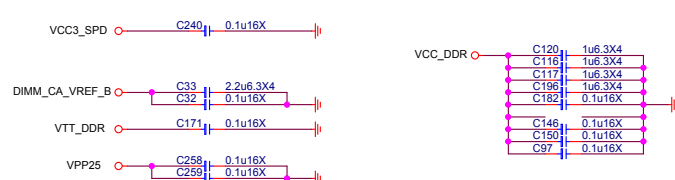
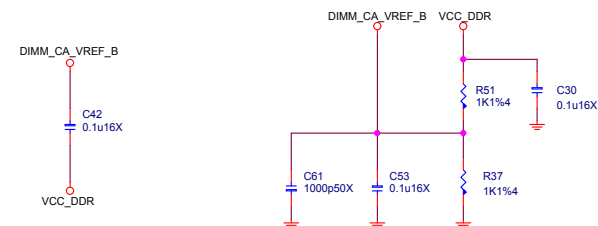
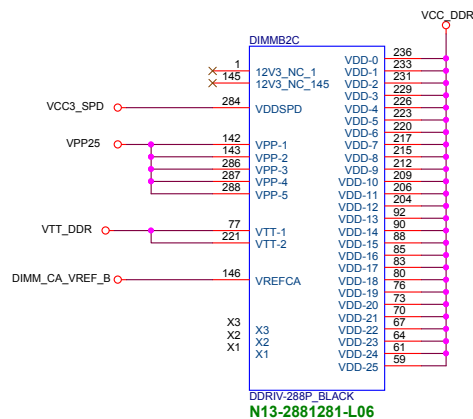
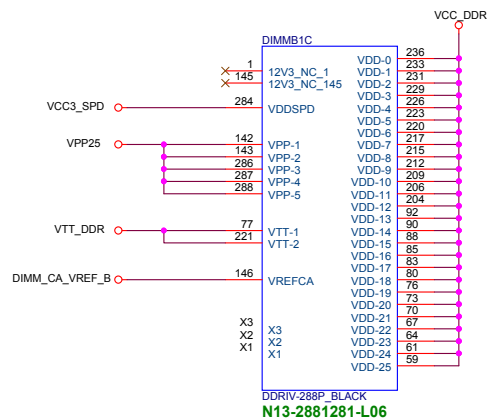
(place resistors close to DIMMs)



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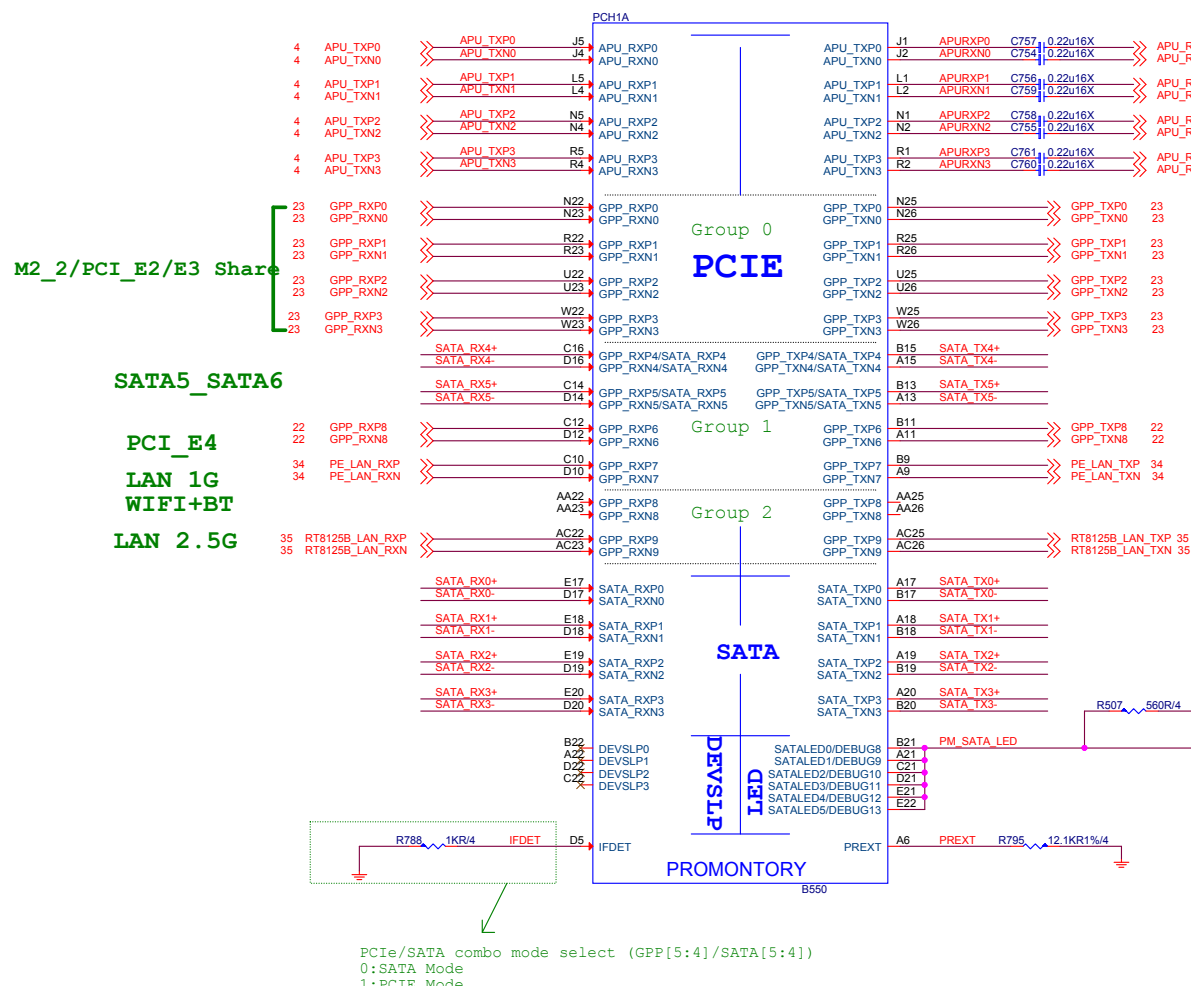
MS-7C91

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<b>MS-7C91</b>			
Size Custom	Document Description <b>DDR4 - POWER/GND-2</b>		Rev 20
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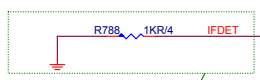




M2\_2/PCI\_E2/E3 Share

SATA5\_SATA6

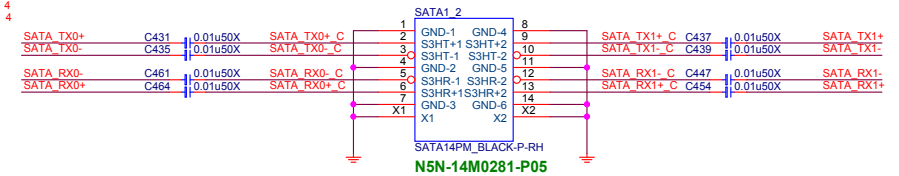
PCI\_E4  
LAN 1G  
WIFI+BT  
LAN 2.5G



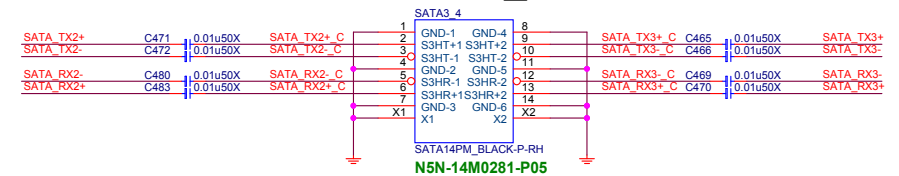
PCie/SATA combo mode select (GPP[5:4]/SATA[5:4])  
0:SATA Mode  
1:PCIE Mode

## SATA Connector

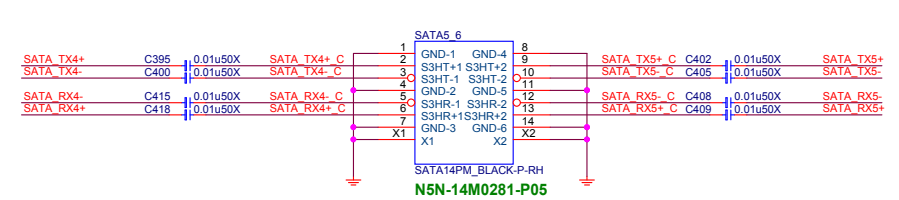
### SATA1\_2

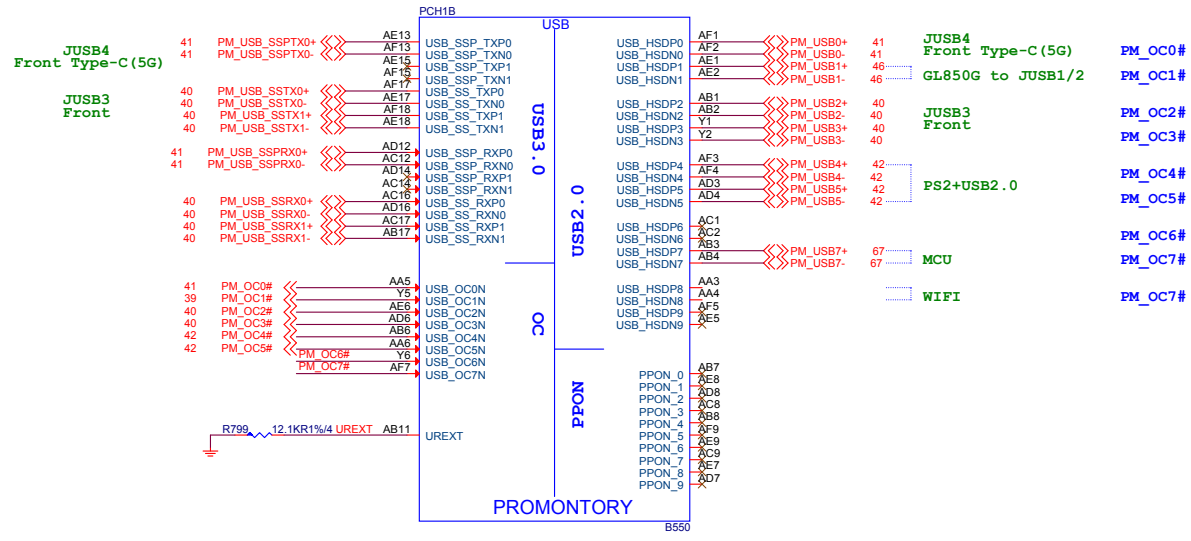


### SATA3\_4



### SATA5\_6

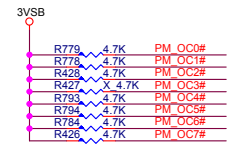


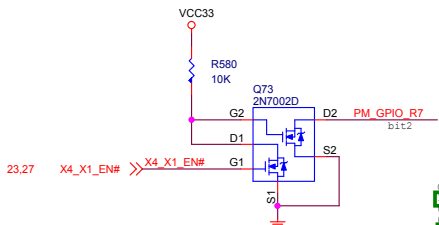


USB mapping

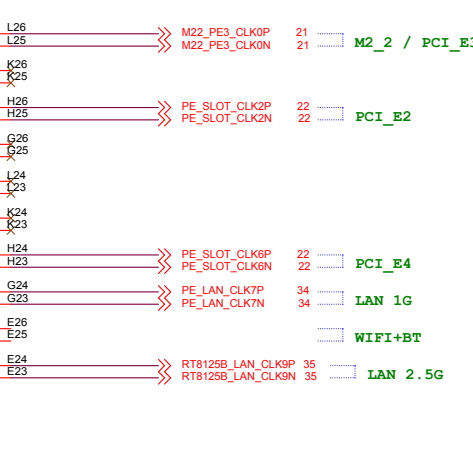
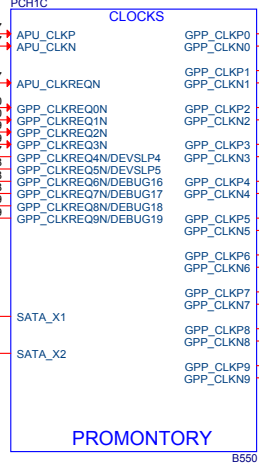
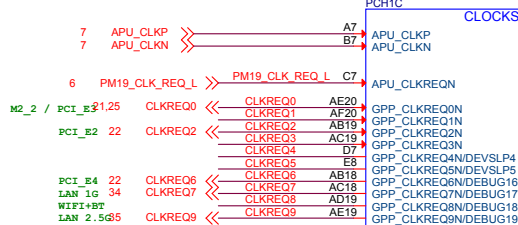
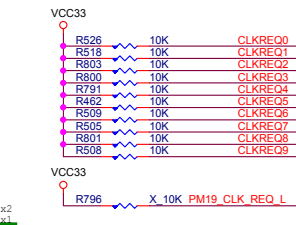
USB\_SSP\_TX/RX[0] + USB\_HSDP/N[0] + USB\_OC0N  
USB\_SSP\_TX/RX[1] + USB\_HSDP/N[1] + USB\_OC1N

USB\_SS\_TX/RX[0] + USB\_HSDP/N[2] + USB\_OC2N  
USB\_SS\_TX/RX[1] + USB\_HSDP/N[3] + USB\_OC3N  
USB\_HSDP/N[4] + USB\_OC4N  
USB\_HSDP/N[5] + USB\_OC5N  
USB\_HSDP/N[6] + USB\_OC6N  
USB\_HSDP/N[7] + USB\_OC7N  
USB\_HSDP/N[8] + USB\_OC7N  
USB\_HSDP/N[9] + USB\_OC7N



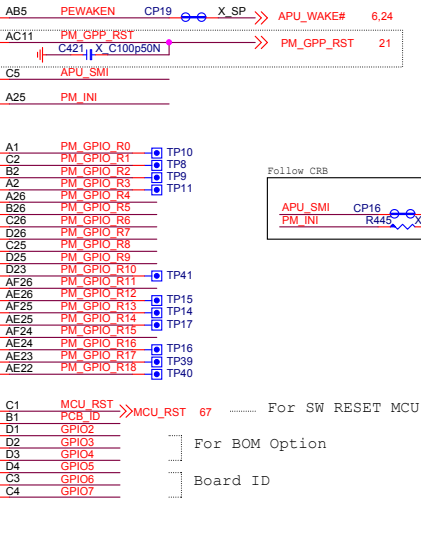
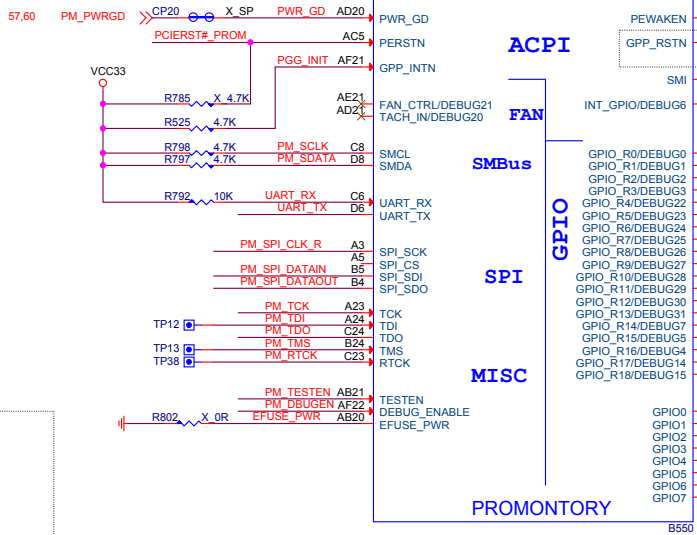
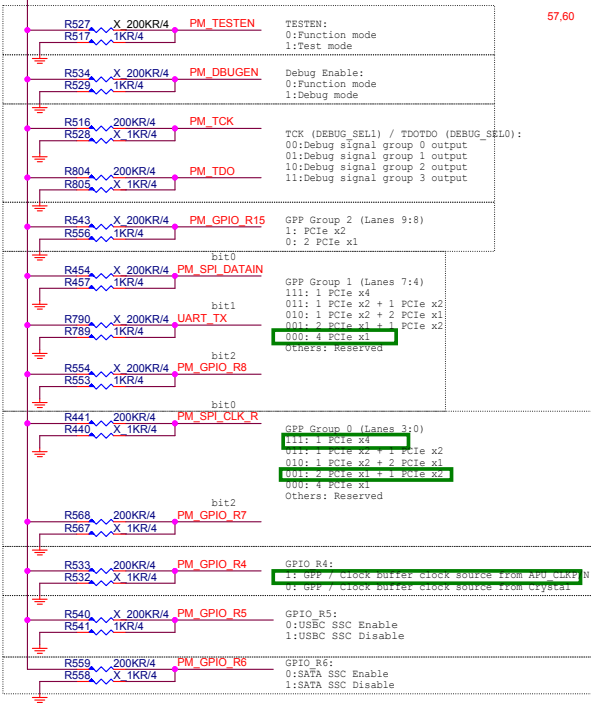


GPP Group 0 (Lanes 3:0)  
111: 1 PCIe x4  
011: 1 PCIe x2 + 1 PCIe x2  
010: 1 PCIe x2 + 2 PCIe x1  
001: 2 PCIe x1 + 1 PCIe x2  
000: 4 PCIe x1  
Others: Reserved

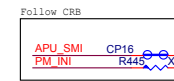


## Strap Information

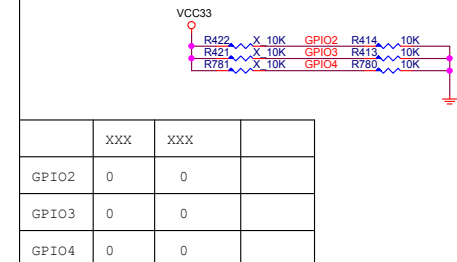
Vih = 2V  
Vil = 0.8V  
Voh = 2.4V  
Vol = 0.4V



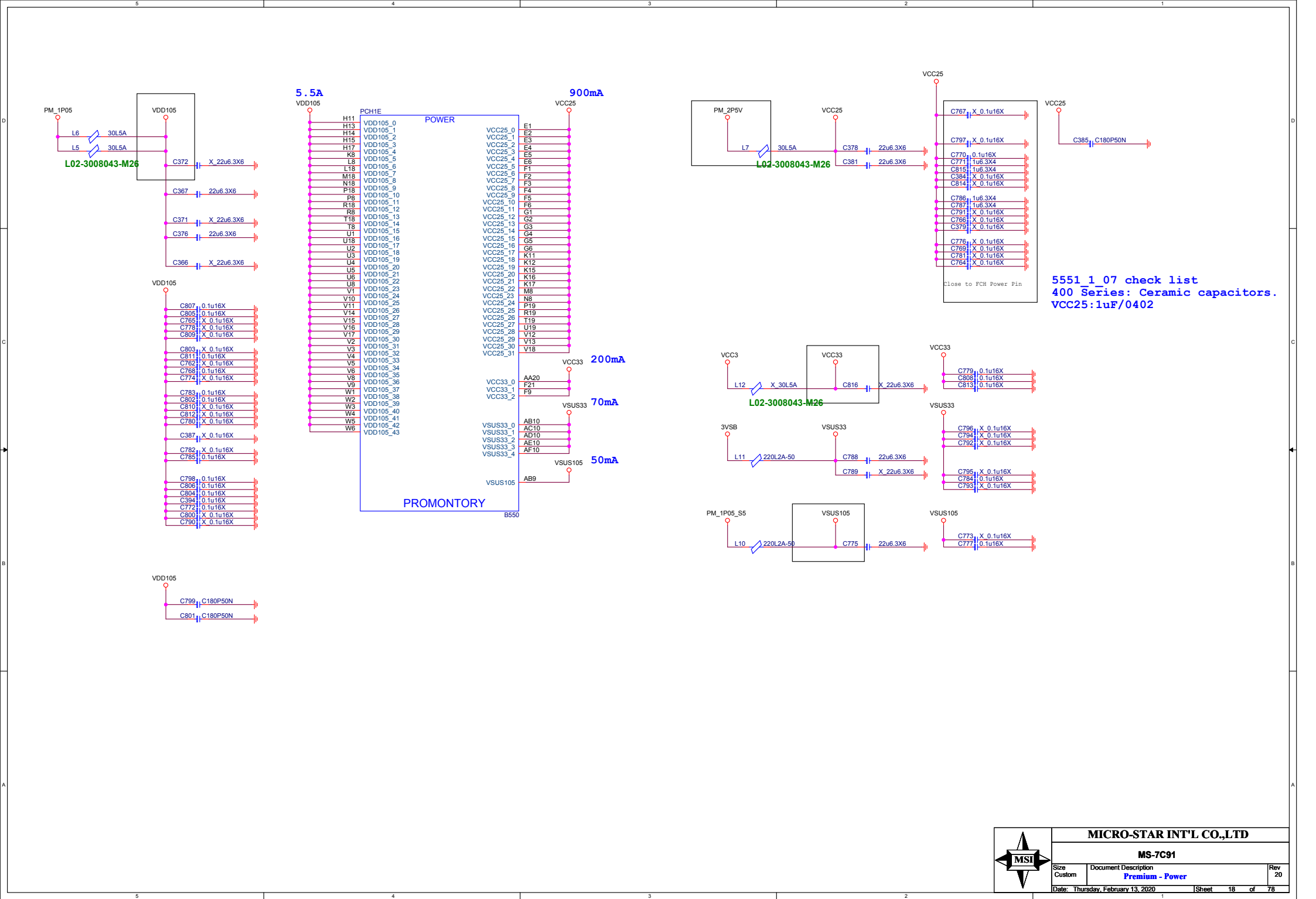
Co-lay GPP\_RSTN Reset for meet FCH sequence. See 55553.



## BOM OPTION



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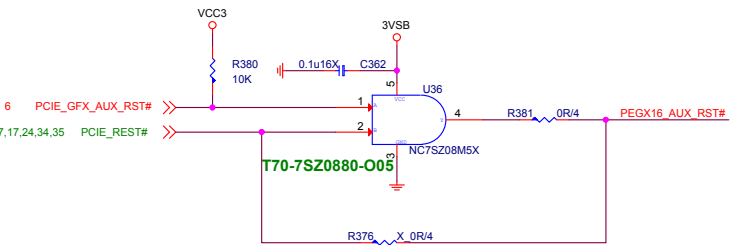
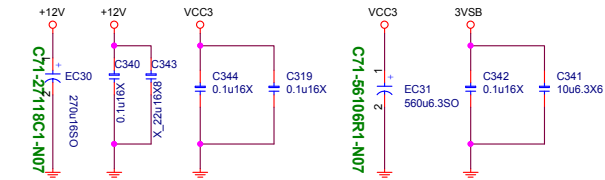
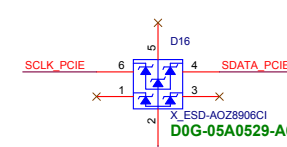
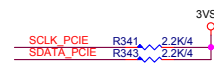




# PCI EXPRESS x16 Slot

## PCI\_E1

SMB\_SEL  
GPIO Default High



### PCI Express x16 Slot

+12V	- 5.5 A
+VCC3	- 3A
+3V3_S5 (wake)	- 375mA
+3V3_S5 (no wake)	- 20mA



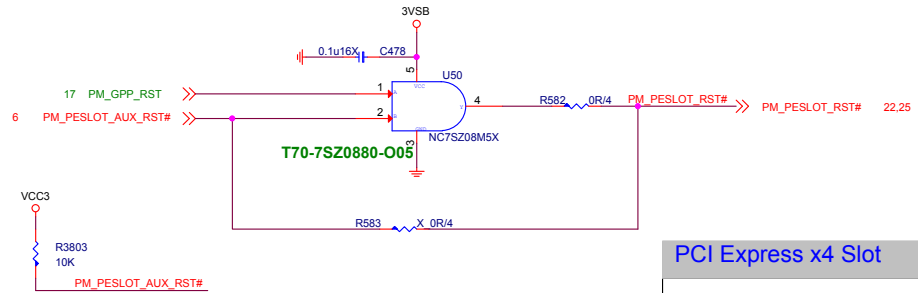
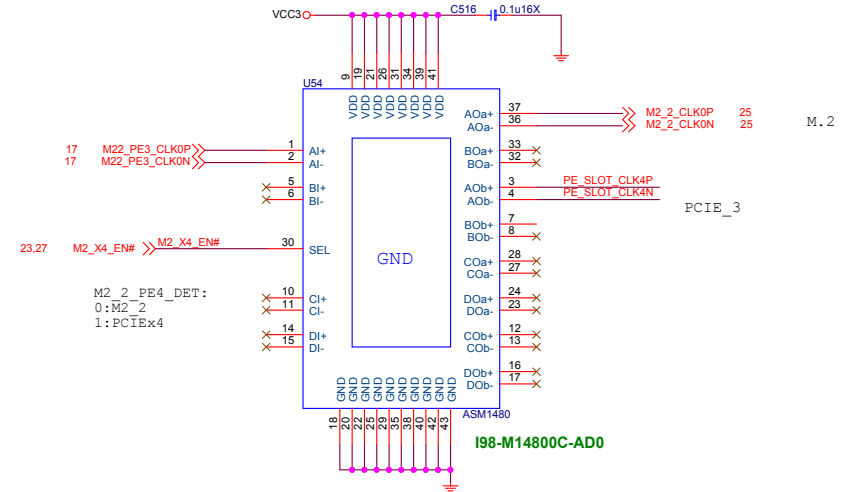
MICRO-STAR INT'L CO.,LTD

MS-7C91

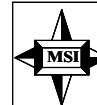
Size	Document Description	Rev
Custom	PCI_E2 (X16)	20
Date: Thursday, February 13, 2020	Sheet 20 of 78	



PCI\_E3 X4



+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA



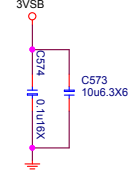
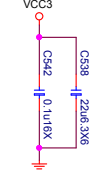
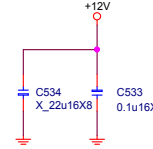
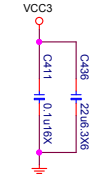
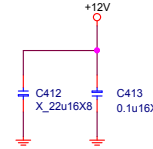
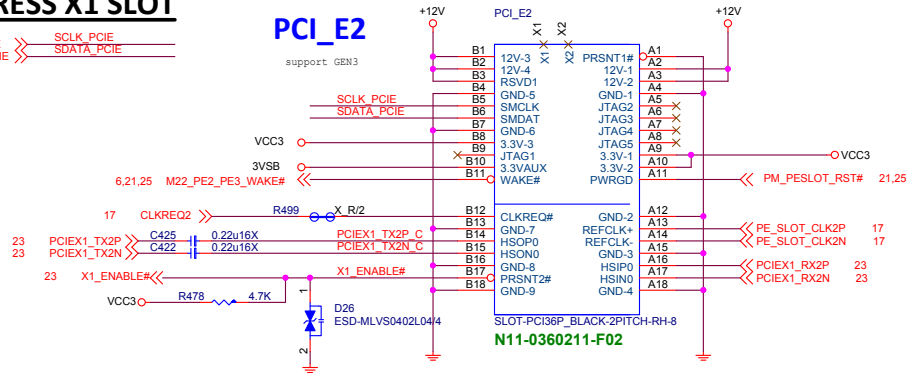
Size Custom	Document Description <b>PCI_E3 (X4)</b>	Rev 20
Date: Thursday, February 13, 2020		Sheet 21 of 78

# PCI EXPRESS X1 SLOT

20,21 SCLK\_PCIE >>> SCLK\_PCIE  
20,21 SDATA\_PCIE >>> SDATA\_PCIE

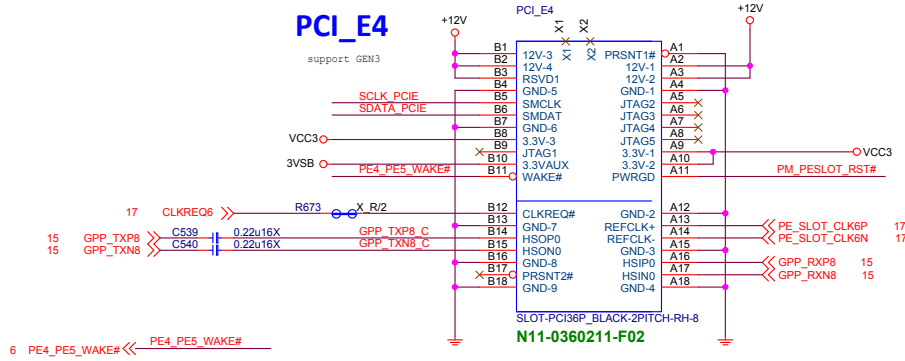
## PCI\_E2

support GEN3




## PCI\_E4

support GEN3



PCI Express x1 Slot *3	
+12V	- 1.5 A
+VCC3	- 9A
+3V3_S5 (wake)	- 1.125A
+3V3_S5 (no wake)	- 20mA

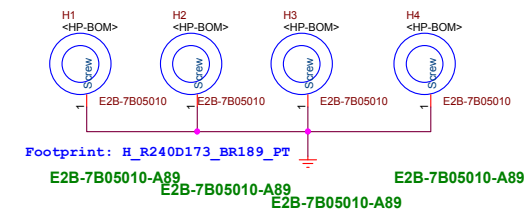


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MS-7C91		
Size Custom	Document Description	Rev 20
PCI_E2/E4_X1		
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VCC3 4.25A  
Max: 14W

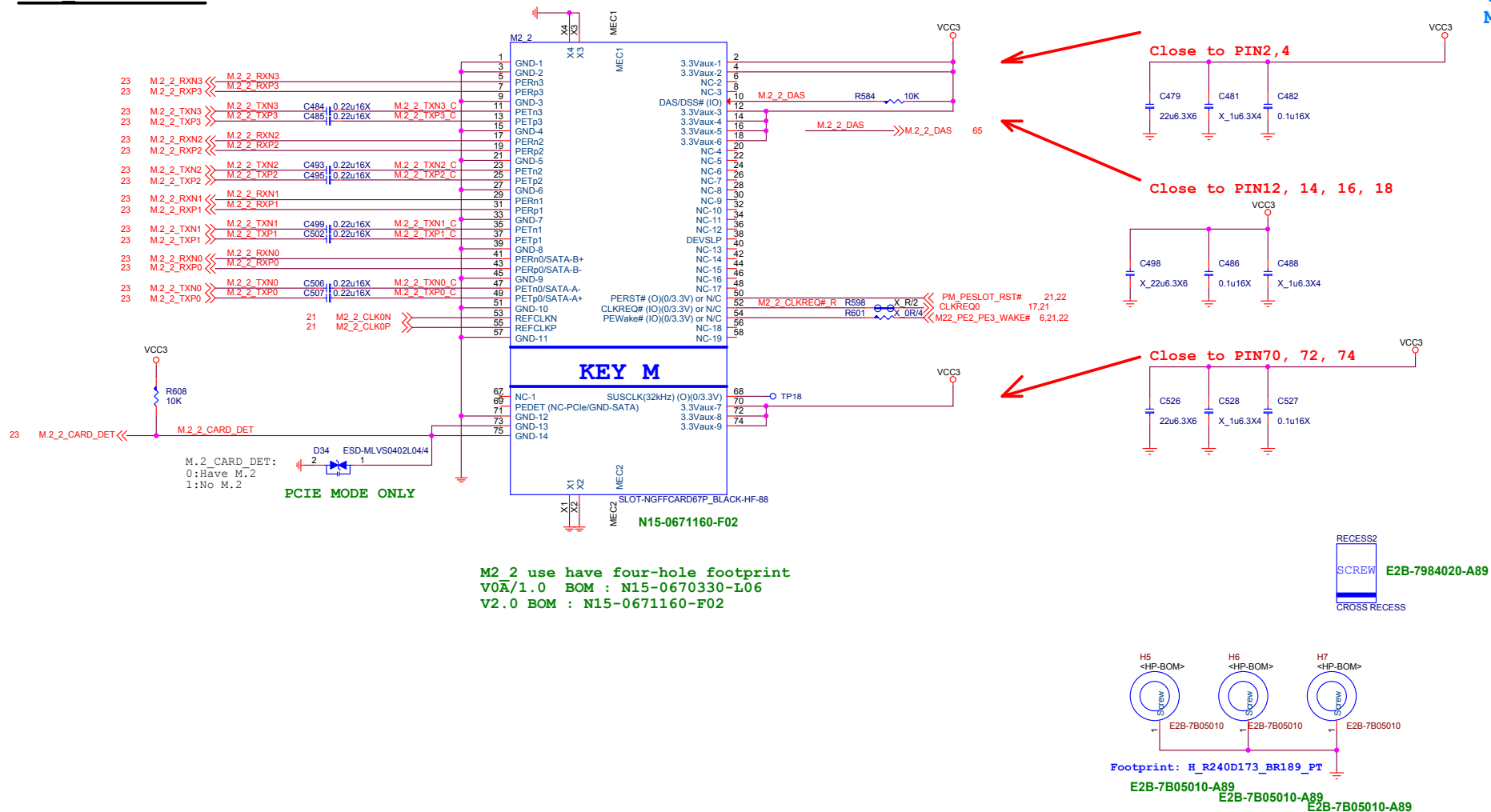
LANE REVERSE TO SUPPORT SATA SSD



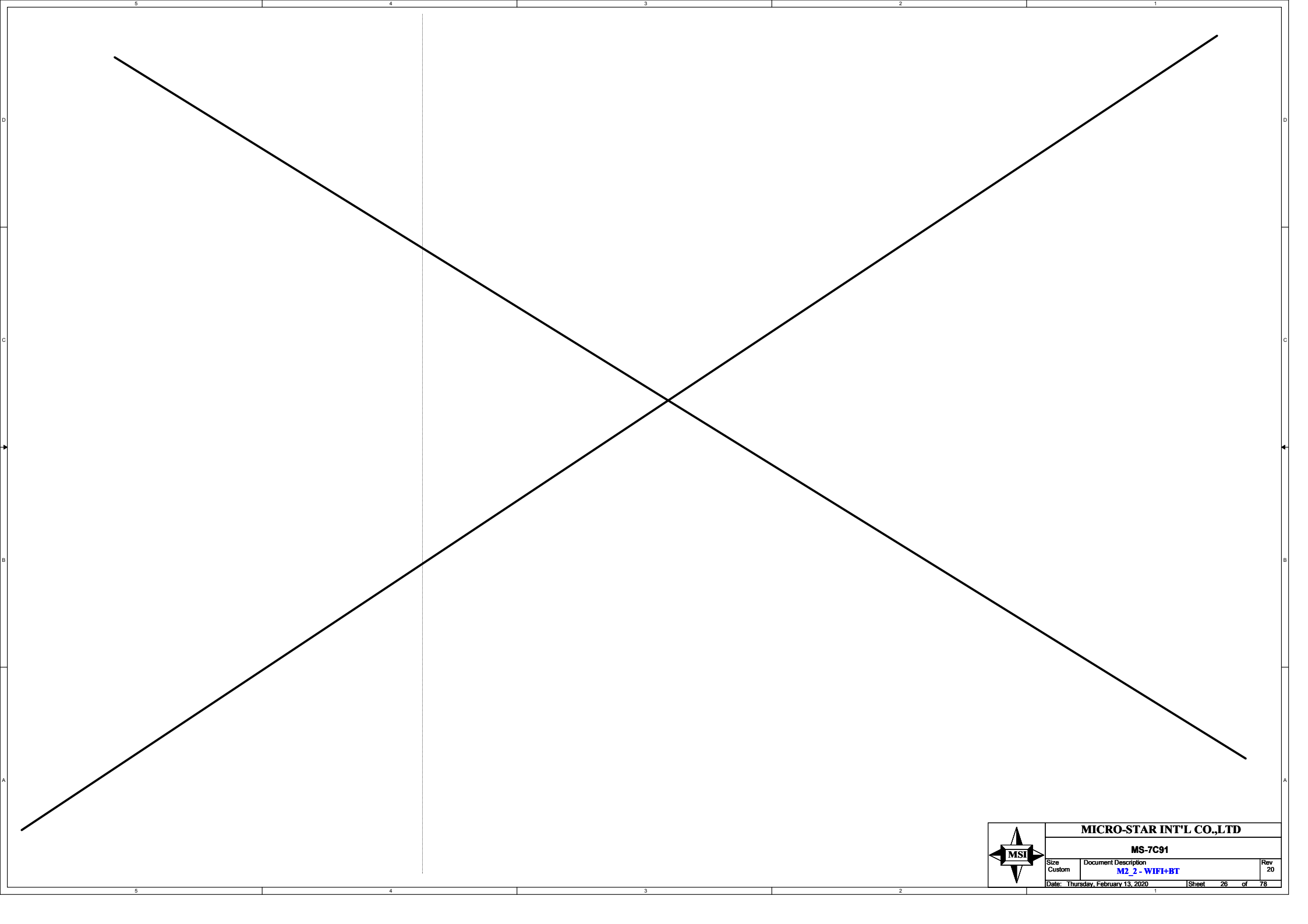
## M.2 2 Connector


M2下方零件擺放限高要小於0.9mm的零件

VCC3 4.25A  
Max: 14W

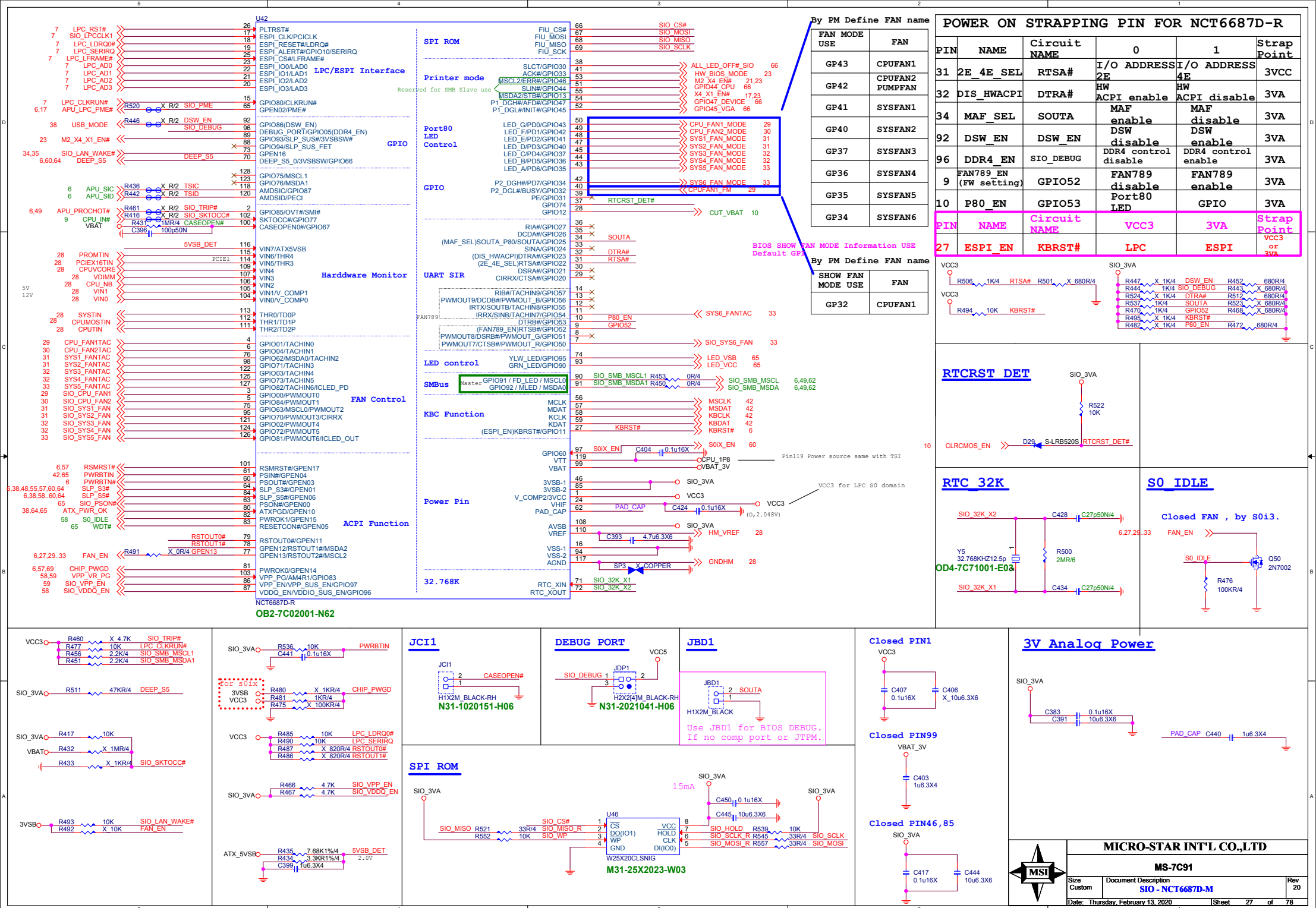


M2 2 use have four-hole footprint  
V0A/1.0 BOM : N15-0670330-L06  
V2.0 BOM : N15-0671160-F02



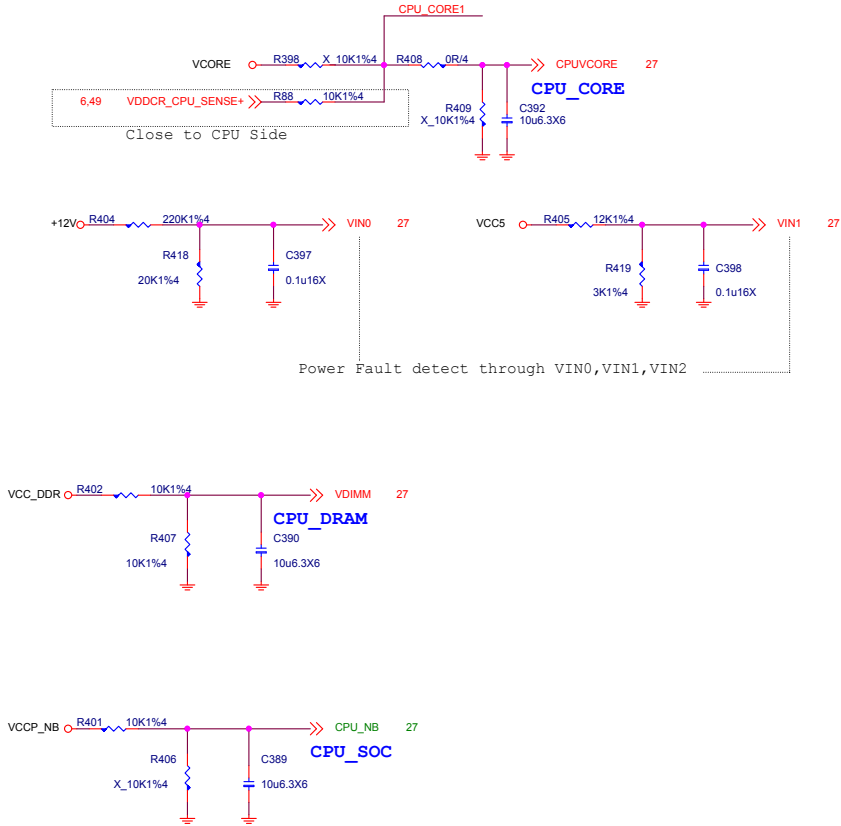
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	<b>MS-7C91</b>		
	Size Custom	Document Description <b>M2_2 - WIFI+BT</b>	Rev 20
Date: Thursday, February 13, 2020		Sheet 26 of 78	



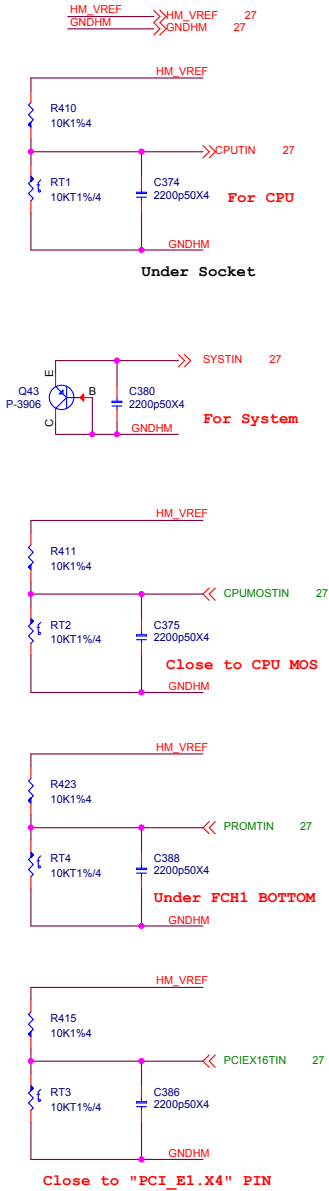


HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect



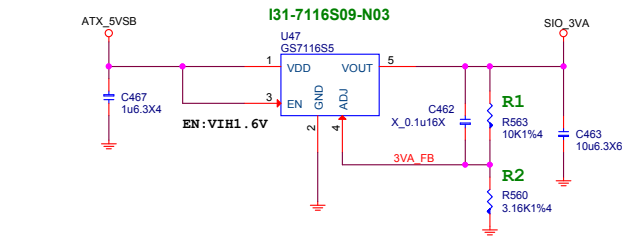
TEMP SENSOR



PM RESET

CPU RESET

SIO\_3VA

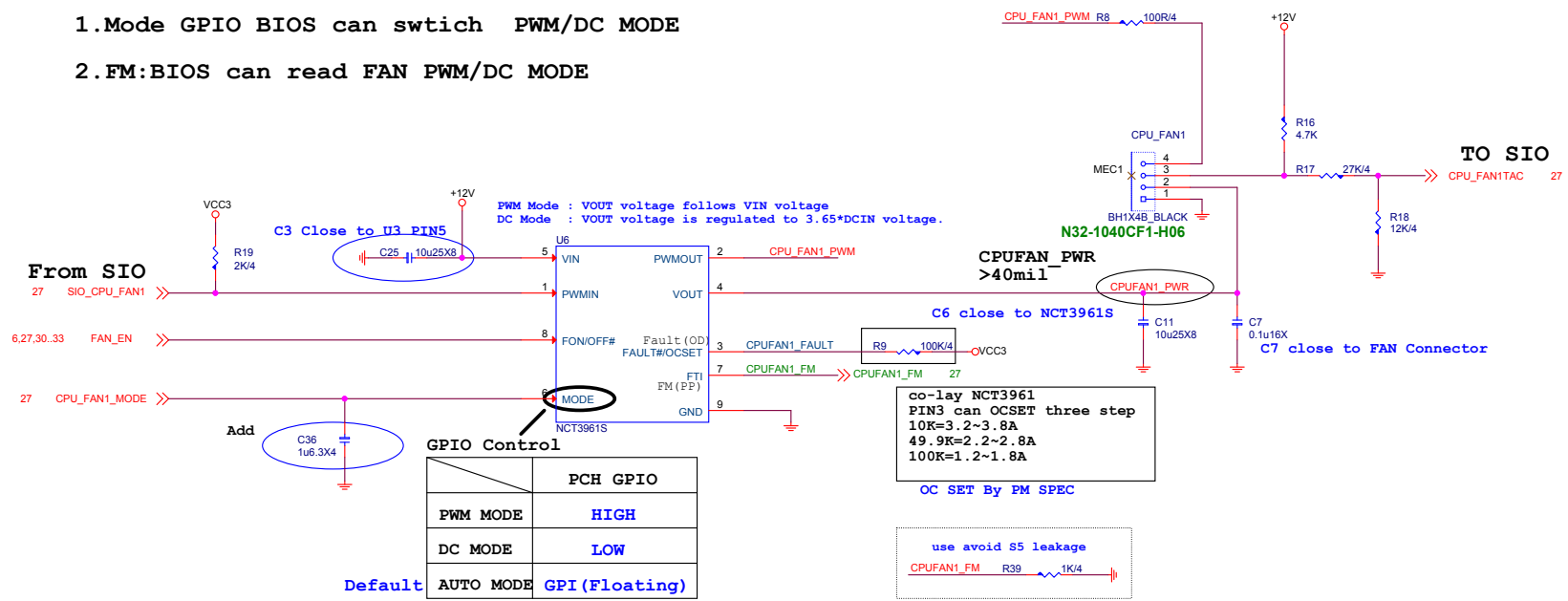


$$V_{out} = V_{ref} * (1 + (R1/R2))$$
$$= 0.8 * (1 + (10K/3.16K))$$
$$= 3.33V$$

MICRO-STAR INT'L CO.,LTD		
MS-7C91		
Size	Document Description	Rev
Custom	SIO - HW Monitor	20
Date: Thursday, February 13, 2020		
Sheet 28 of 78		

CPUFAN1 TYPE N : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

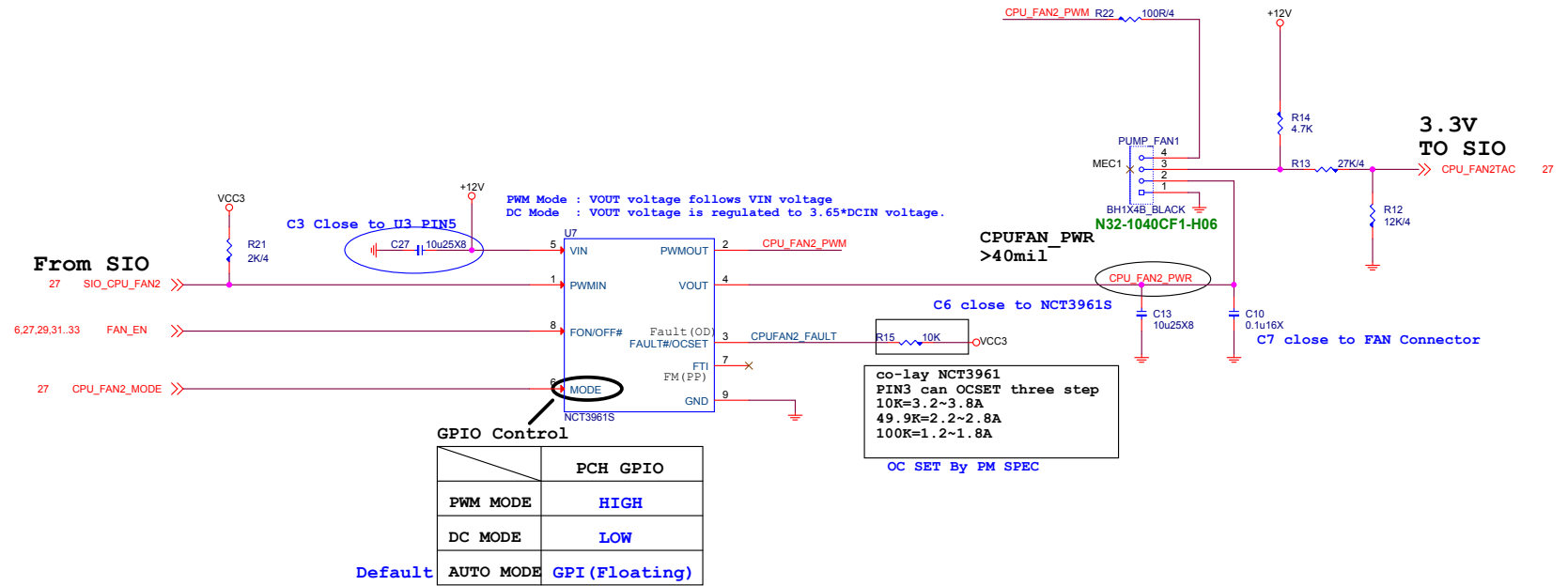
- 1.Mode GPIO BIOS can swtich PWM/DC MODE
- 2.FM:BIOS can read FAN PWM/DC MODE



# PUMPFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE



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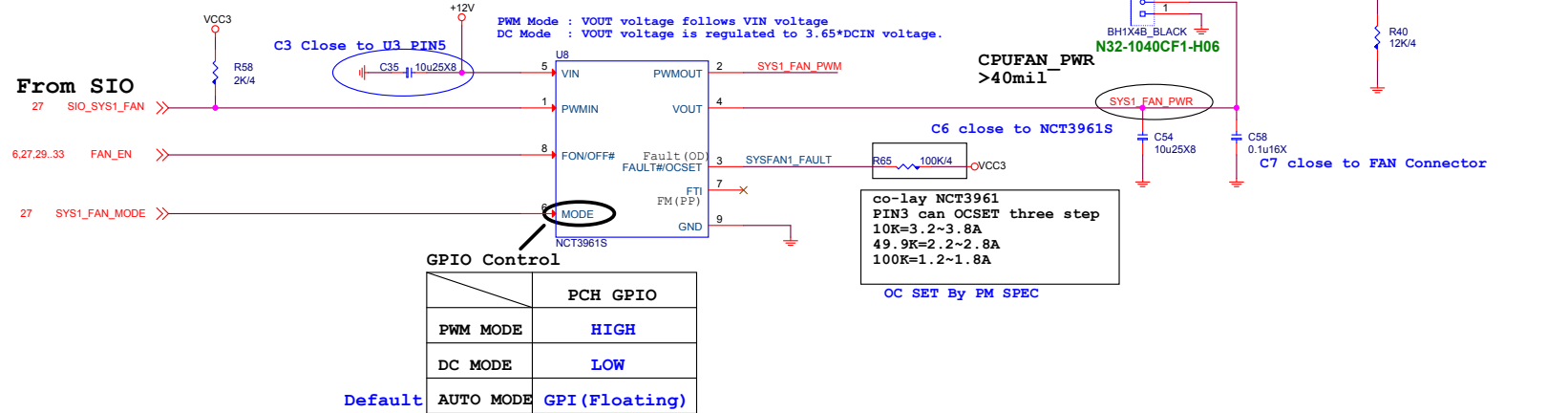
MS-7C91

Size	Document Description	Rev
Custom	FAN TYPE-K PUMPFAN1	20
Date: Thursday, February 13, 2020	Sheet 30 of 78	

# SYSFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

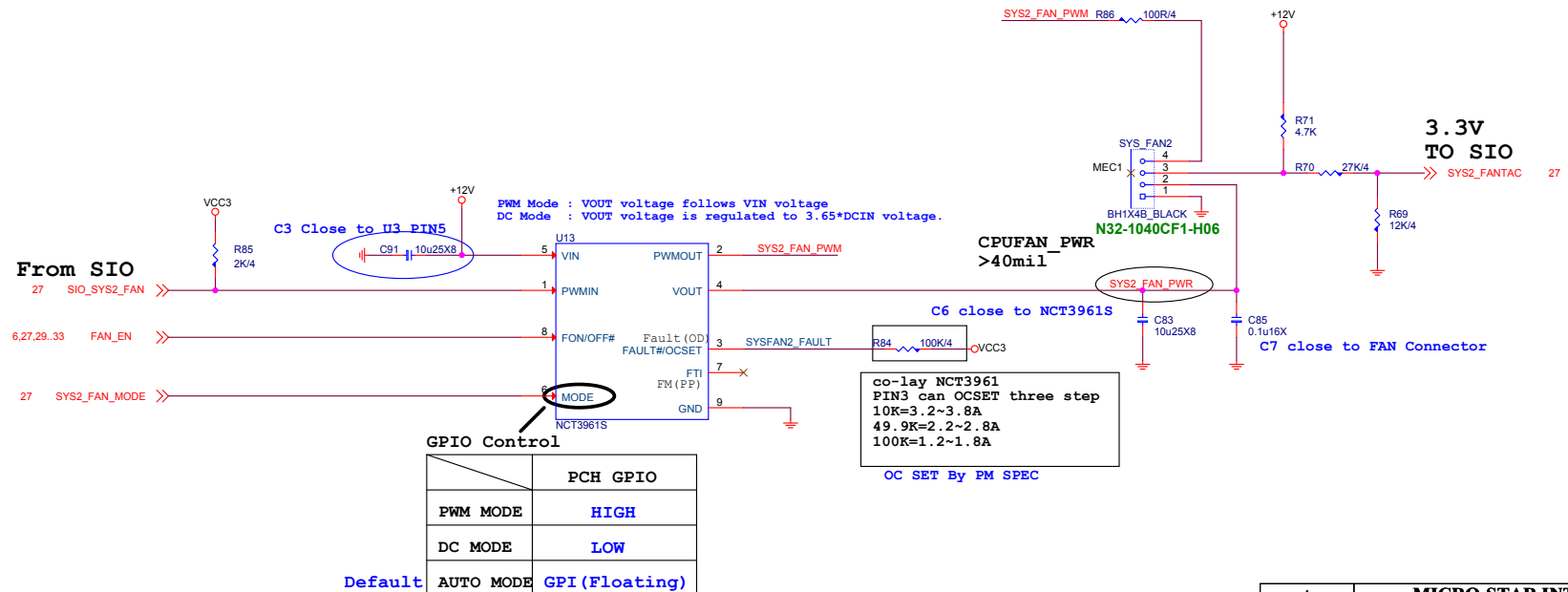
1.Mode GPIO BIOS can swtich PWM/DC MODE



# SYSFAN2

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

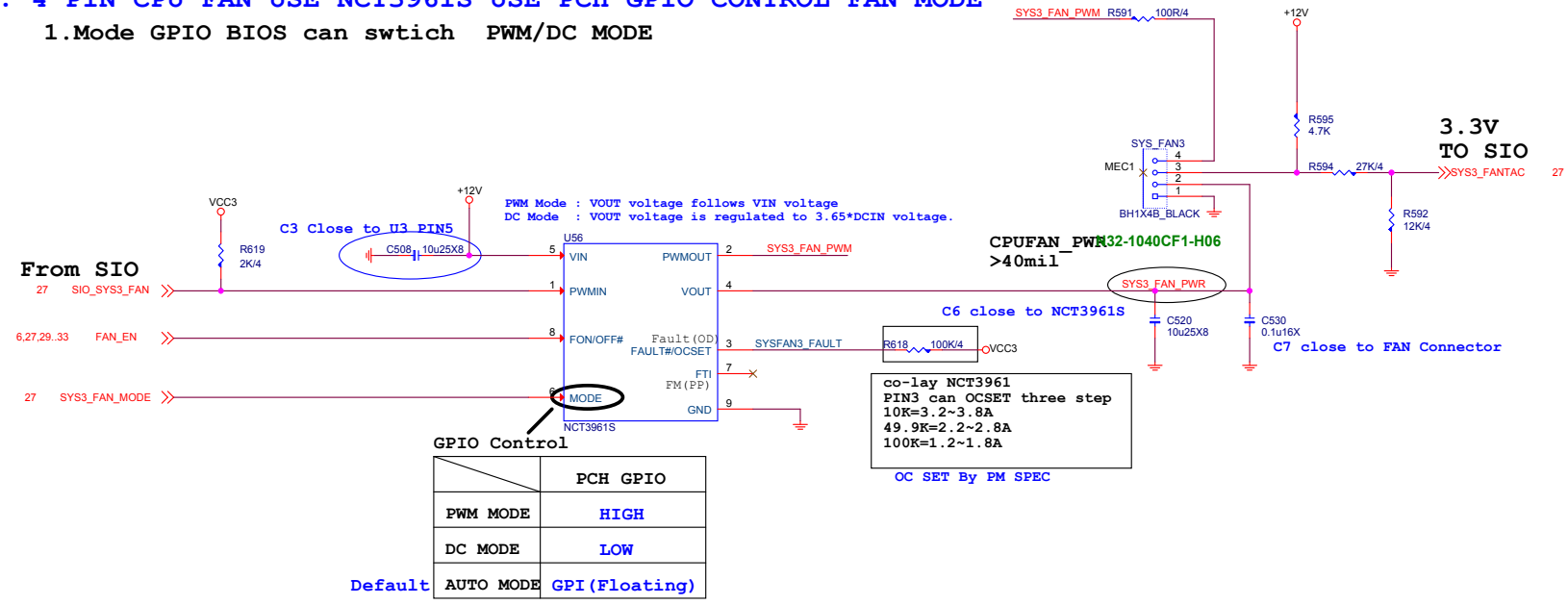
1.Mode GPIO BIOS can swtich PWM/DC MODE



**SYSFAN3**

**TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE**

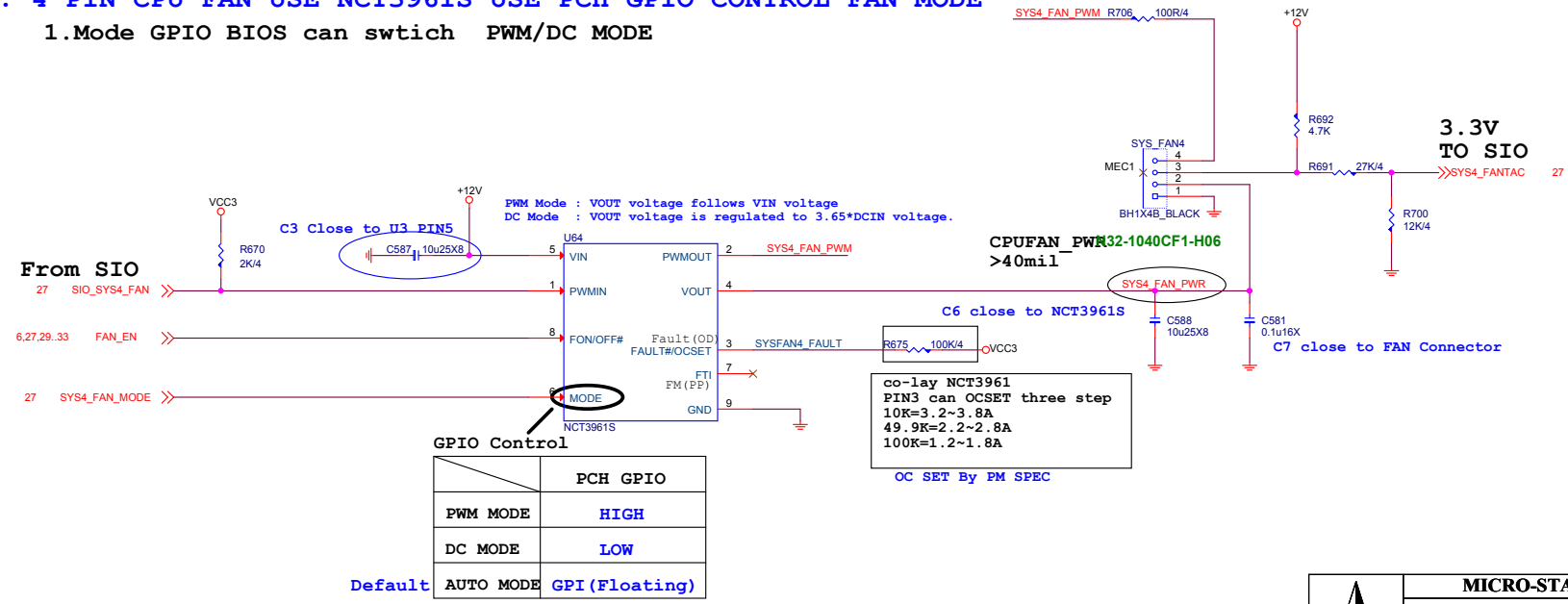
1.Mode GPIO BIOS can swtich PWM/DC MODE



**SYSFAN4**

**TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE**

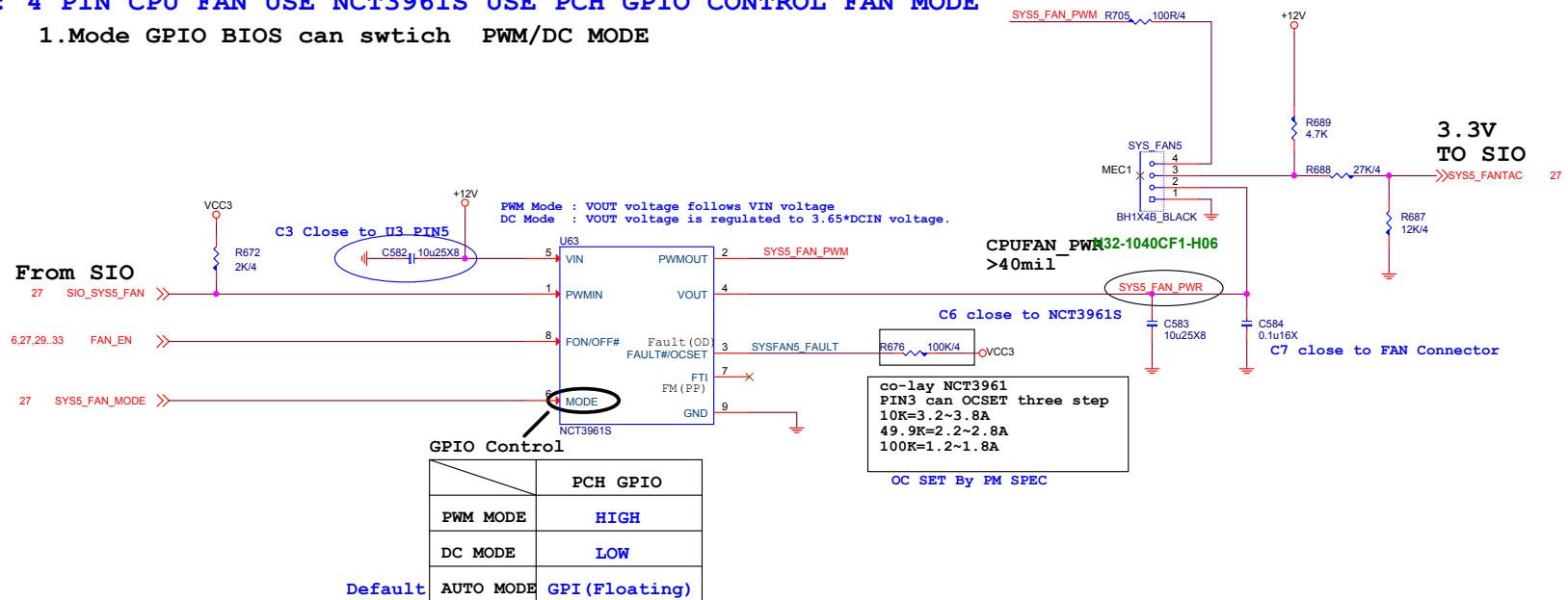
1.Mode GPIO BIOS can swtich PWM/DC MODE





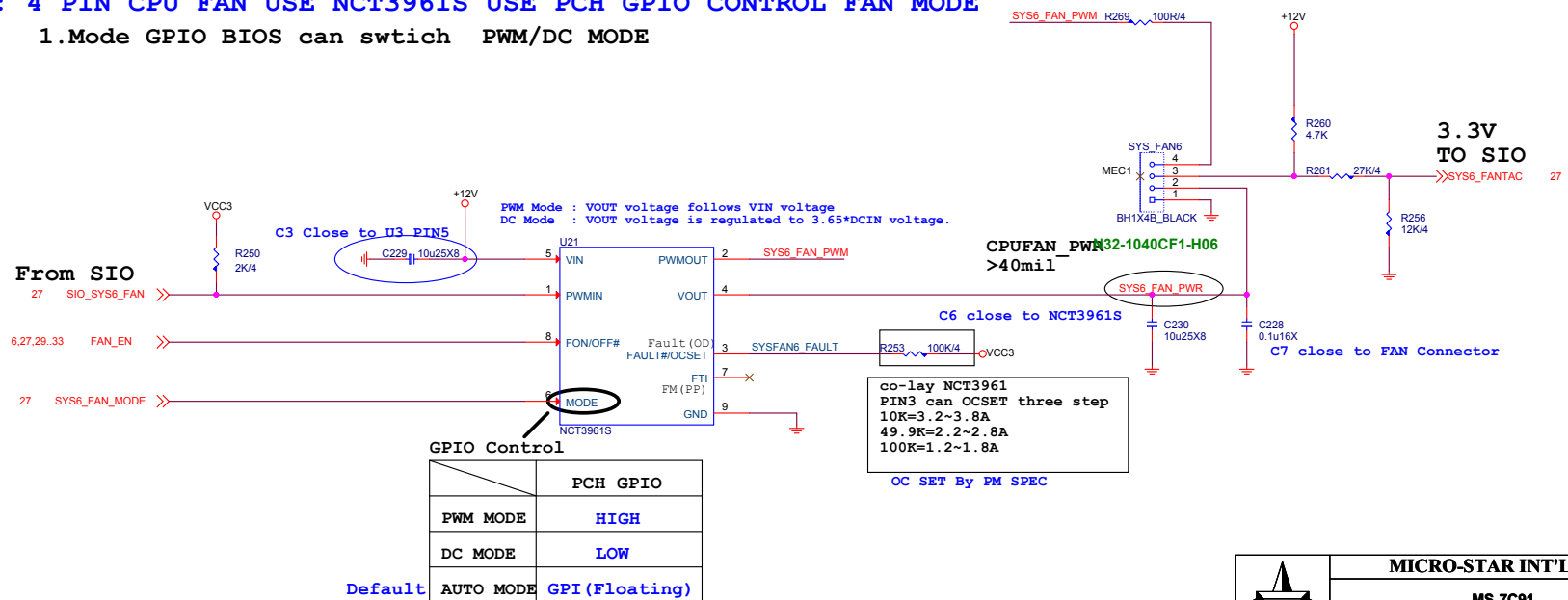
```
SYSFAN5 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE
```

## 1.Mode GPIO BIOS can swtich PWM/DC MODE



```
SYSFAN6 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE
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### 1.Mode GPIO BIOS can swtich PWM/DC MODE

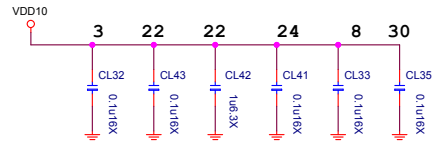
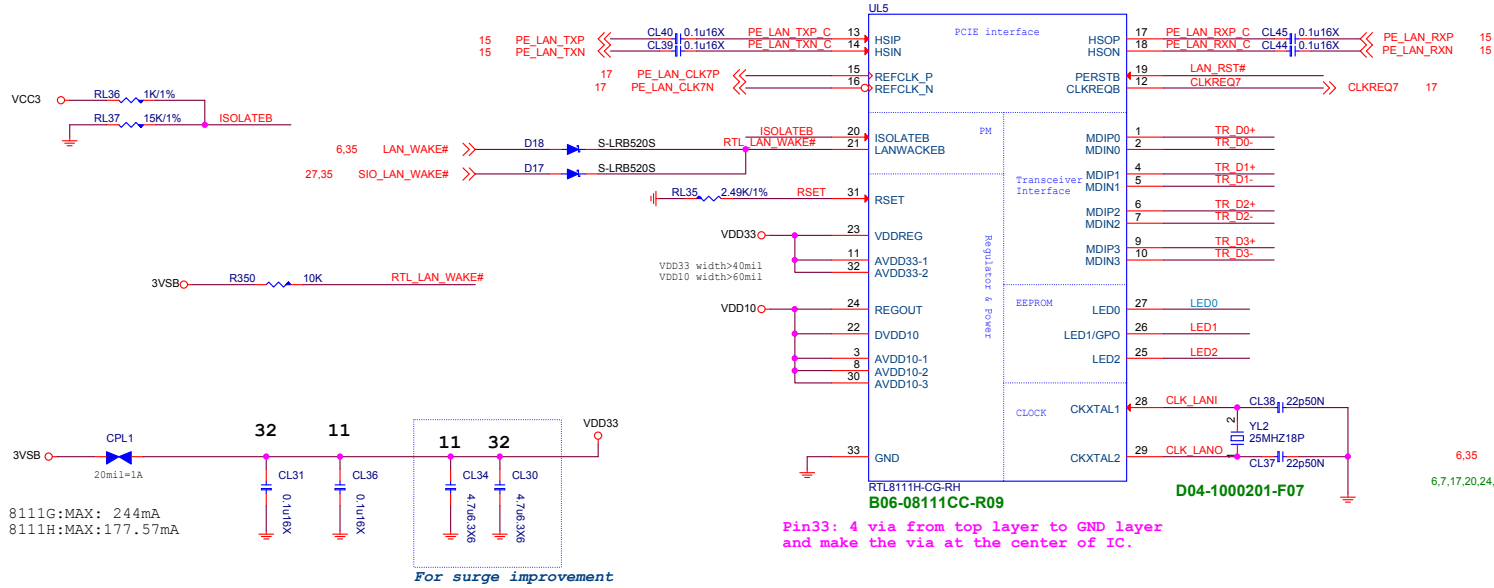


**MICRO-STAR INT'L CO.,LTD**

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Size Custom	Document Description <b>FAN TYPE-N SYSFANS</b>	Rev 20
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## RTL8111H Giga LAN

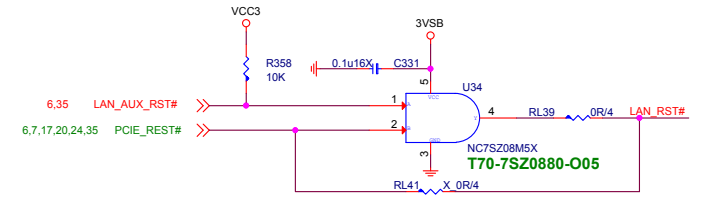
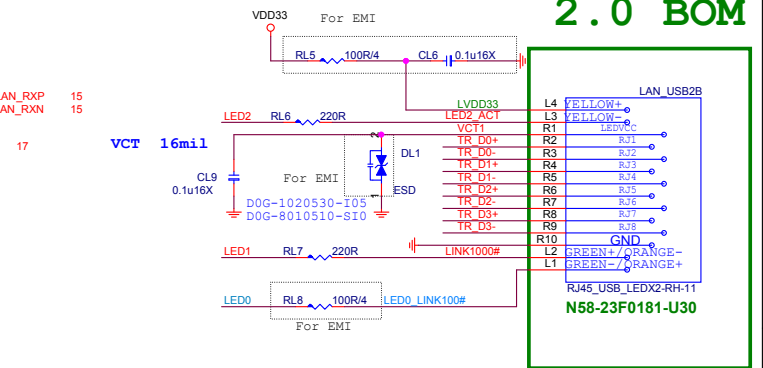


### 8111G POWER Consumption

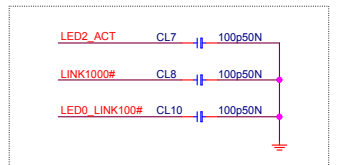
	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

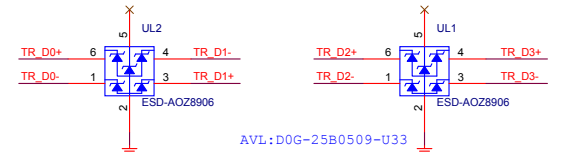
	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
AI DPS	5.50	18.15



For EMI 2015.06.22



ESD Protect  
UL2&UL3 close to connector

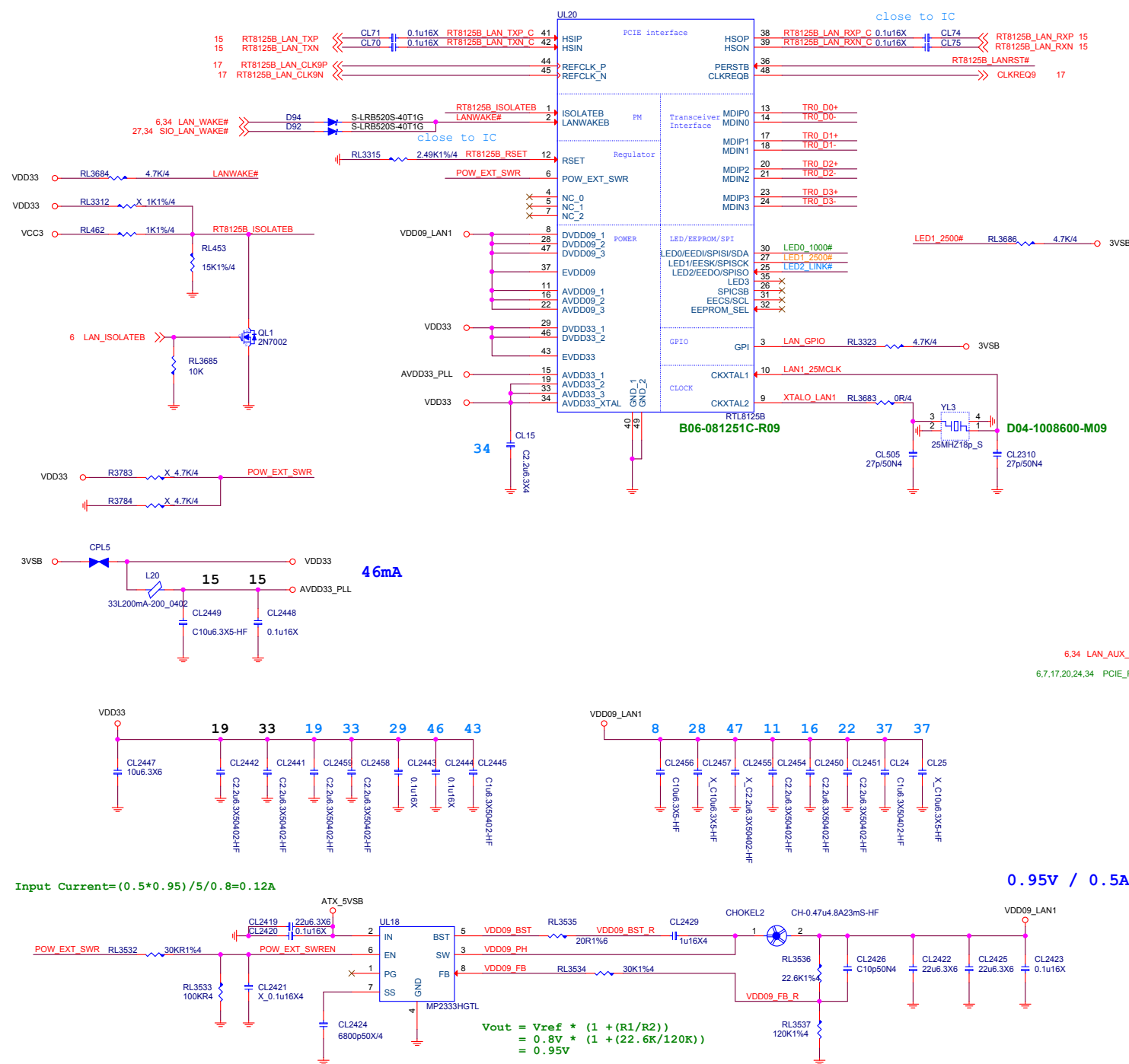


**MICRO-STAR INT'L CO.,LTD**

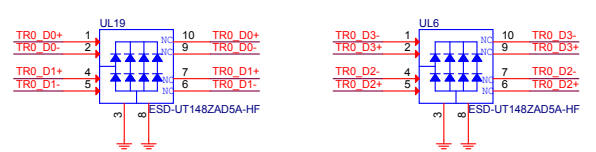
MS-7C91

Size Custom	Document Description <b>RTL8111H Giga LAN</b>	Rev 20
Date: Thursday, February 13, 2020		Sheet 34 of 78

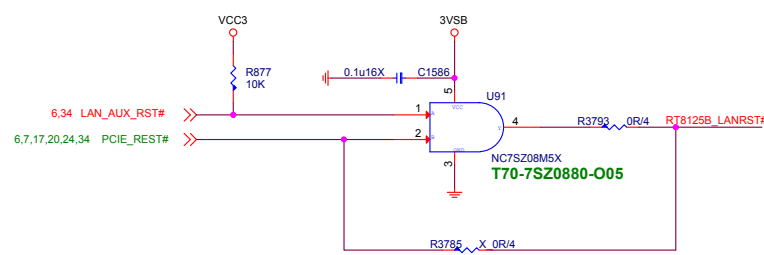
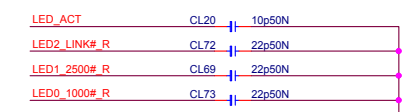
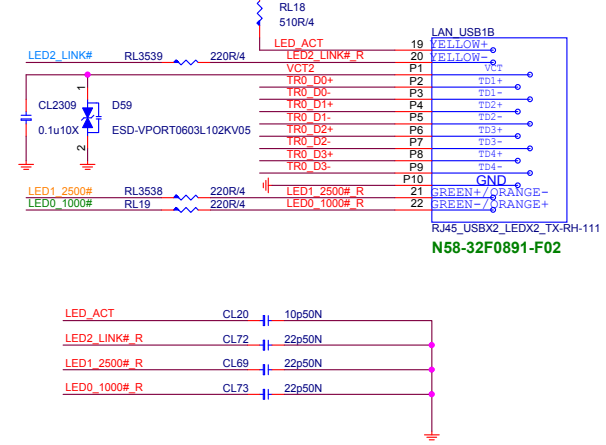
Realtek Lan1-RTL8125B(2.5G)



ESD Protect  
close to connector



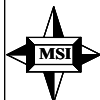
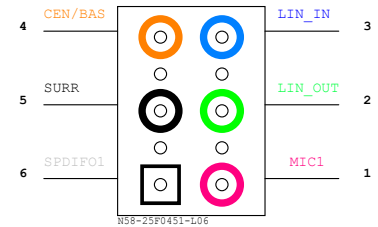
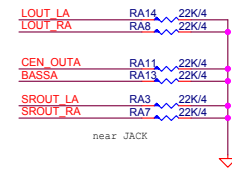
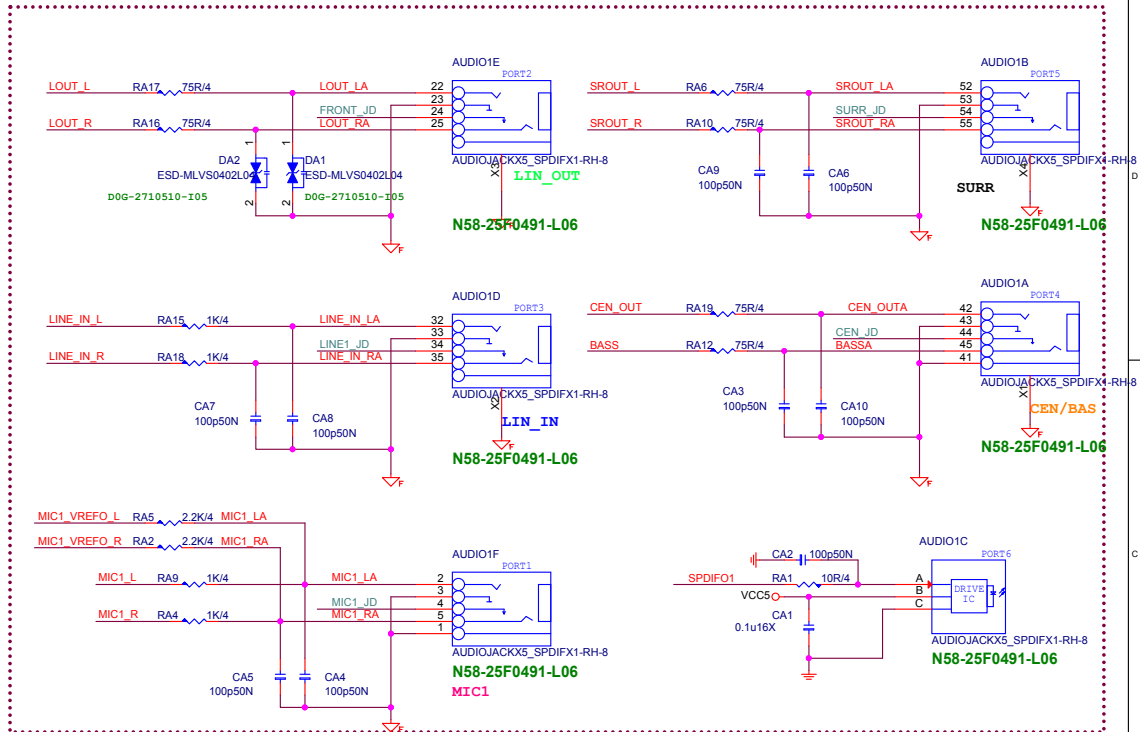
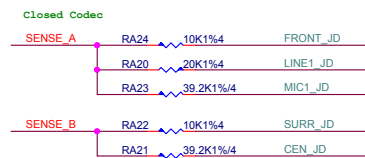
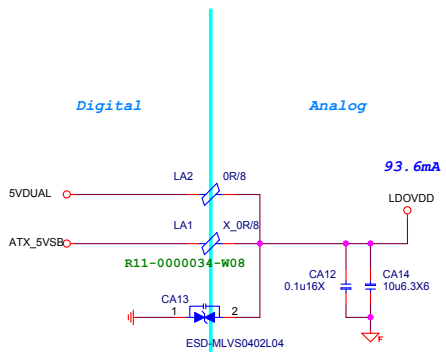
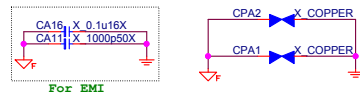
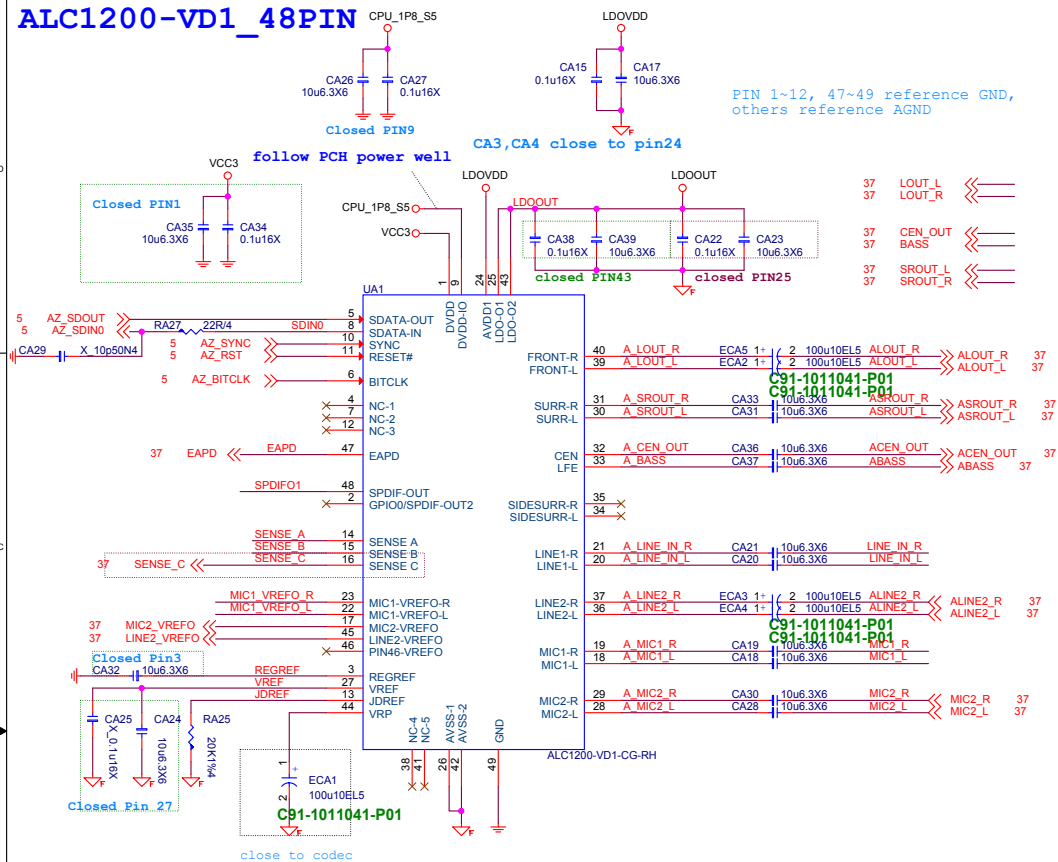
LAN Connector



0.95V / 0.5A

MSI			MICRO-STAR INT'L CO.,LTD		
			MS-7C91		
Size	Custom	Document Description	LAN - RTL8125B		
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			Rev 20		

## ALC1200-VD1 48PIN



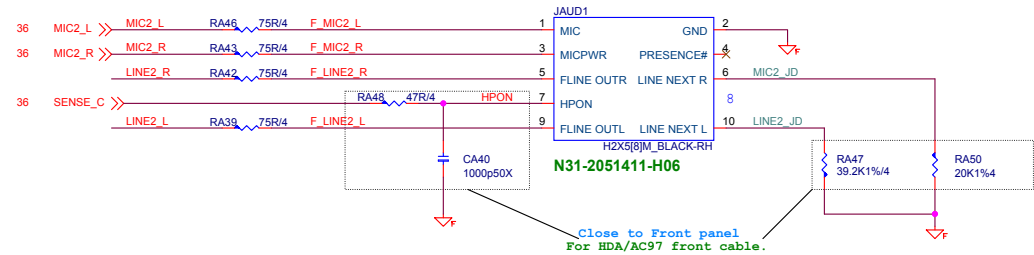
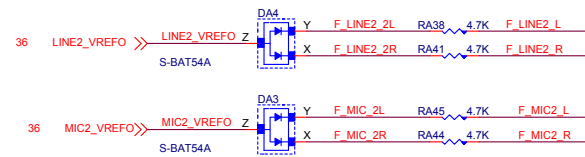
**MICRO-STAR INT'L CO.,LTD**

MS-7C91

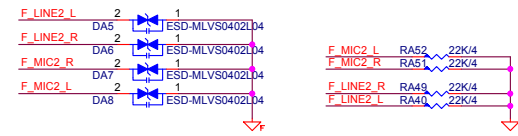
Size Custom	Document Description <b>Audio ALC1200-VD</b>
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Rev  
20

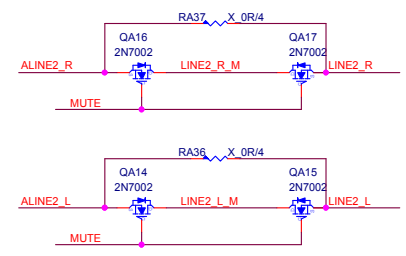
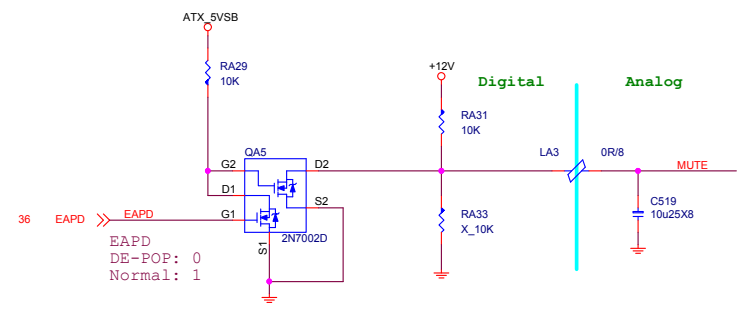
Date: Thursday, February 13, 2020 Sheet 36 of 78



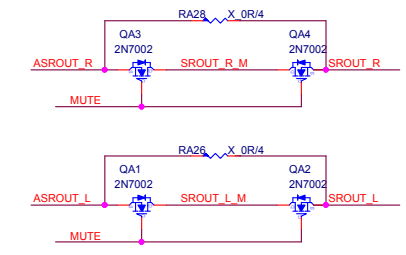
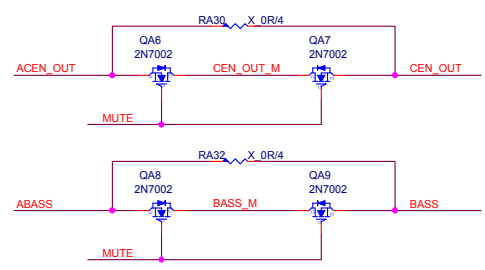
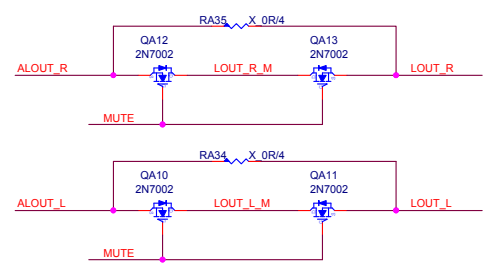
D0G-2710510-I05  
Close to Front panel  
**ESD protect**  
D0G-2710510-I05  
AVL:D0G-2950500-S10



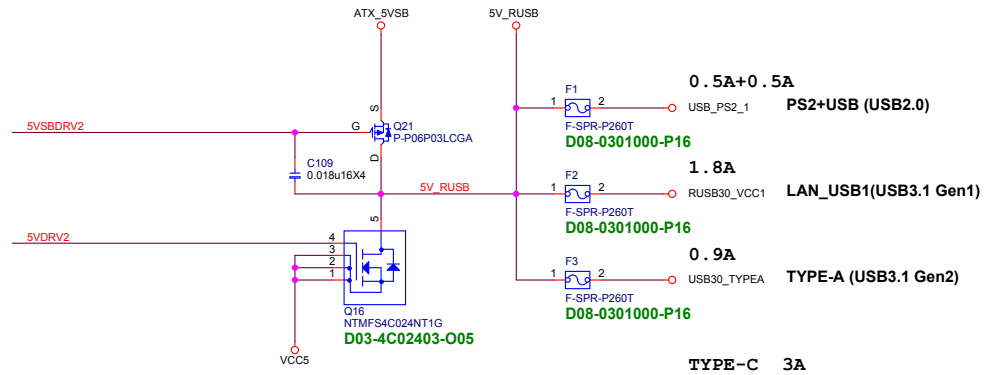
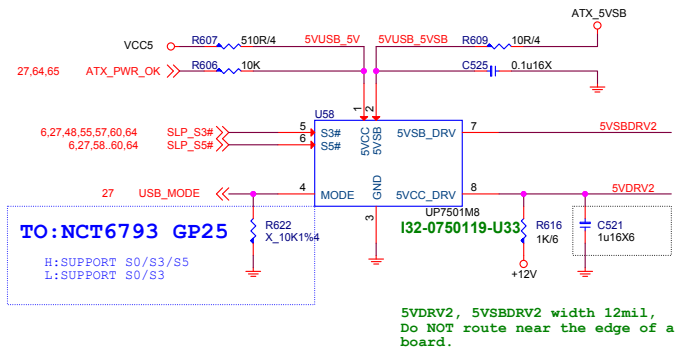
# De-POP circuit



- LOUT\_L 36
- LOUT\_R 36
- SROUT\_L 36
- SROUT\_R 36
- CEN\_OUT 36
- BASS 36
- ALINE2\_R 36
- ALINE2\_L 36
- ALOUT\_R 36
- ALOUT\_L 36
- ASROUT\_R 36
- ASROUT\_L 36
- ACEN\_OUT 36
- ABASS 36

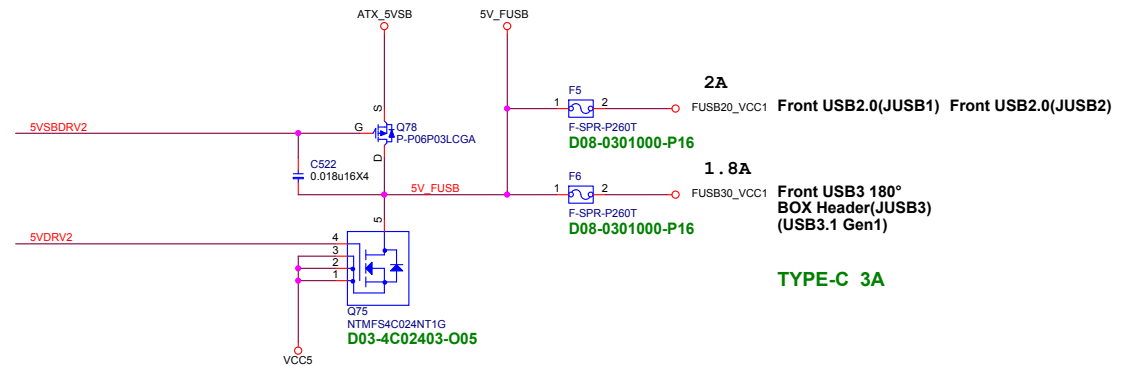


## USB Power



### Rear (6.7A)

**Front (6.8A)**



**MICRO-STAR INT'L CO.,LTD**

MS-7C91

Size Custom	Document Description <b>USB Power - UP750I</b>	Rev 20
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# Front USB2.0 (JUSB2)

Form GL850G USB2.0 HUB

5V@1A

- 46

MB\_USB\_HUB\_3D+

<<>>

MB\_USB\_HUB\_3D+
- 46

MB\_USB\_HUB\_3D-

<<>>

MB\_USB\_HUB\_3D-
- 46

MB\_USB\_HUB\_4D+

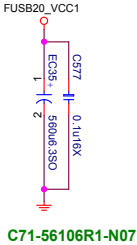
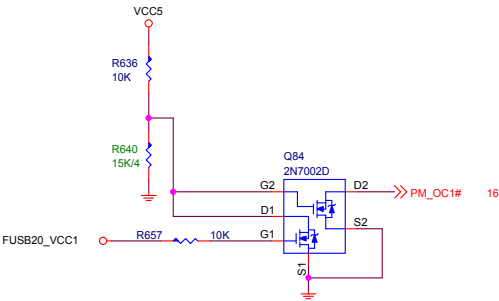
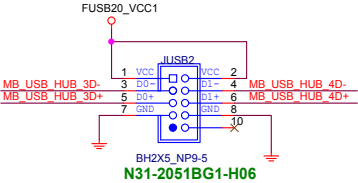
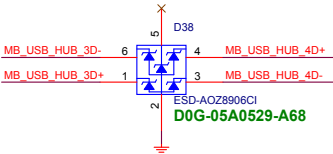
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MB\_USB\_HUB\_4D+
- 46

MB\_USB\_HUB\_4D-

<<>>

MB\_USB\_HUB\_4D-



# Front USB2.0 (JUSB1)

Form GL850G USB2.0 HUB

5V@1A

- 46

MB\_USB\_HUB\_1D+

<<>>

MB\_USB\_HUB\_1D+
- 46

MB\_USB\_HUB\_1D-

<<>>

MB\_USB\_HUB\_1D-
- 46

MB\_USB\_HUB\_2D+

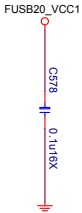
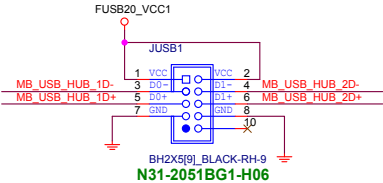
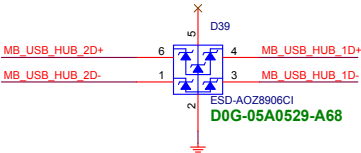
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MB\_USB\_HUB\_2D+
- 46

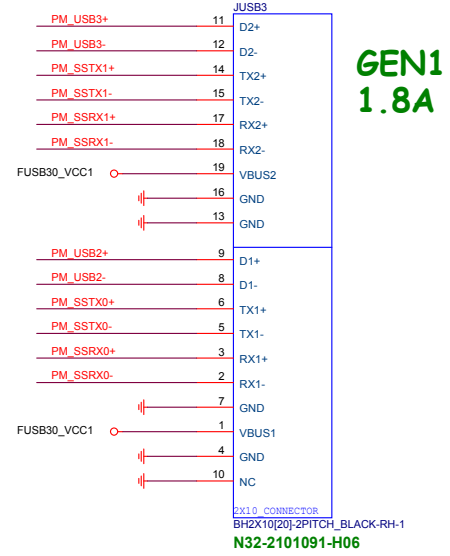
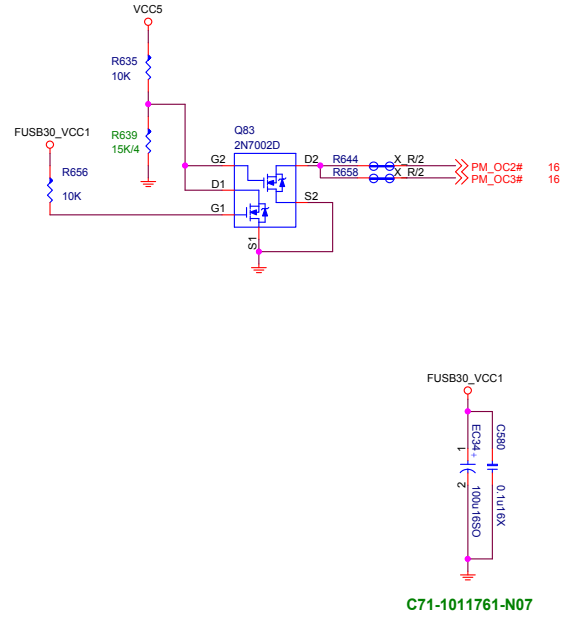
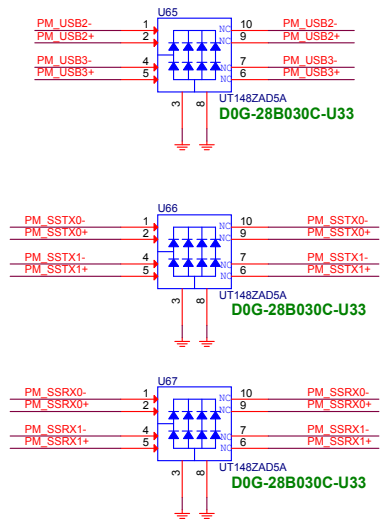
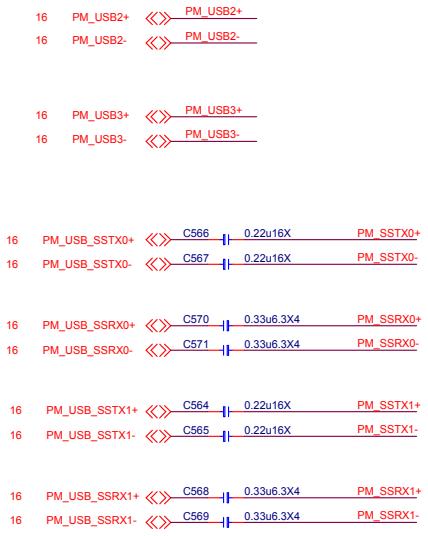
MB\_USB\_HUB\_2D-

<<>>

MB\_USB\_HUB\_2D-



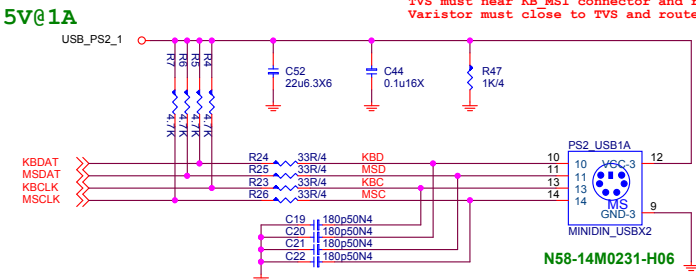
Front USB3 180°  
BOX Header(JUSB3)  
5V@1.8A



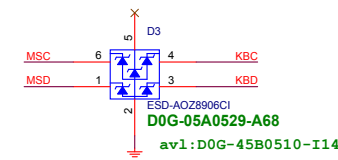




PS2+USB (USB2.0)



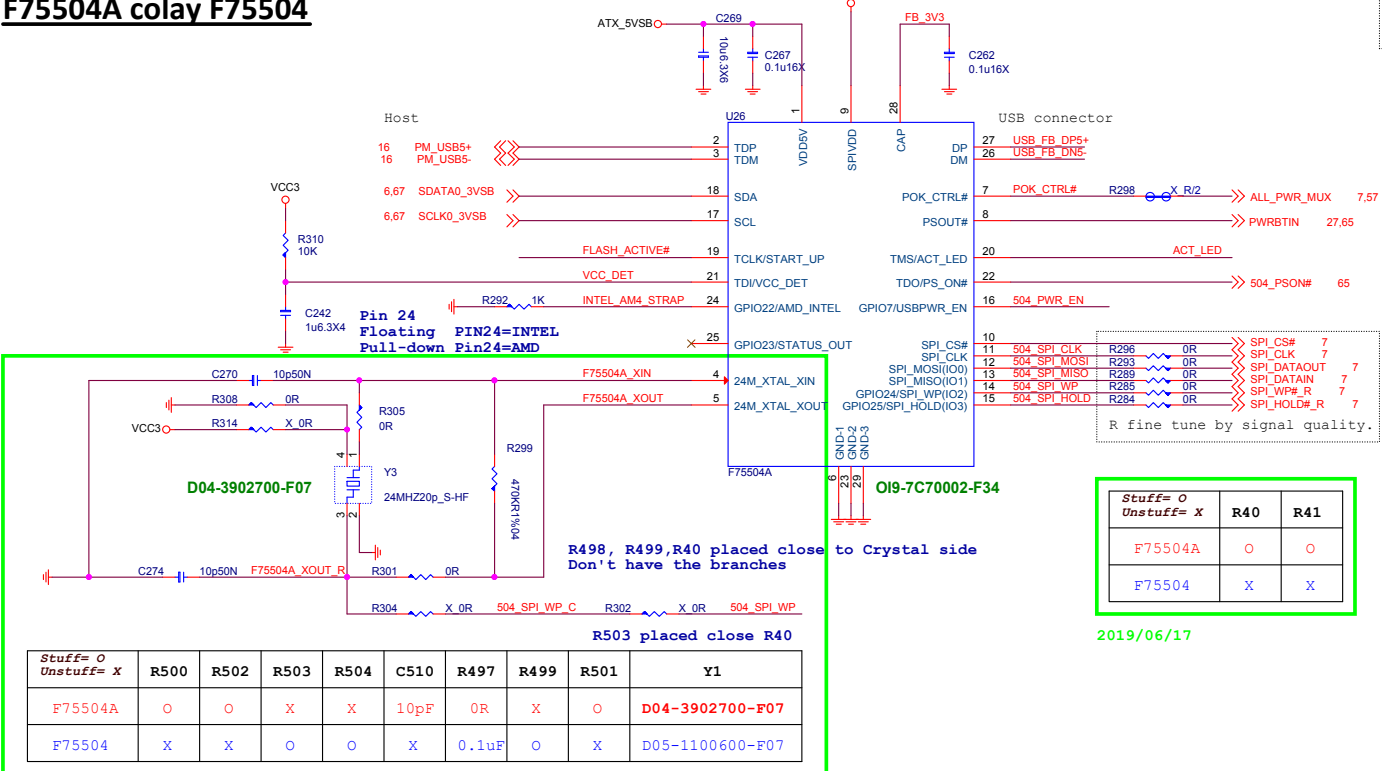
layout note:  
C21 must close to TVS pin5  
TVS must near KB MS1 connector and route without branch  
Varistor must close to TVS and route without branch



USB Flash BIOS

F75504A colay F75504

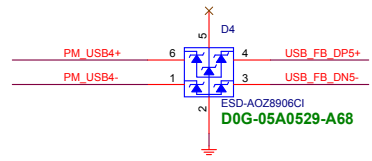
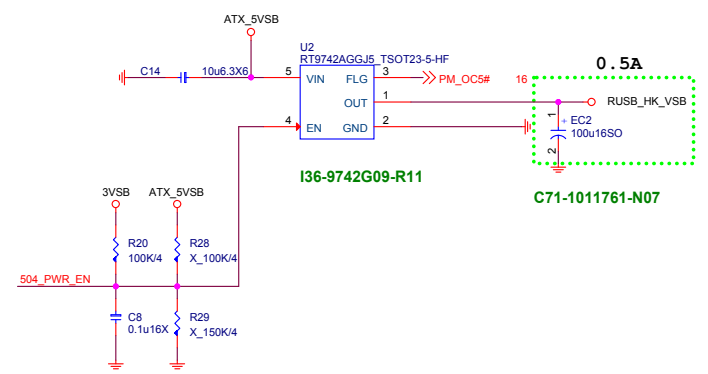
F75504A/F75504 layout placement must meet to spi/usb trace length spec with host.  
As for as possible place near to host.



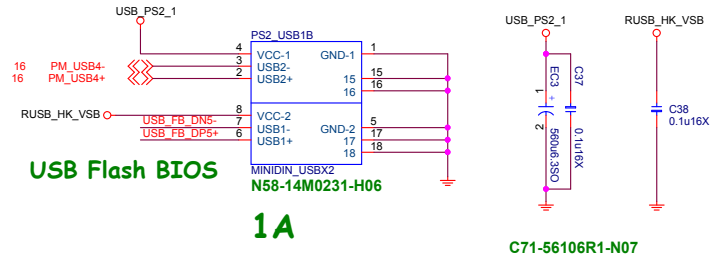
Stuff= 0		
Unstuff= X	R40	R41
F75504A	0	0
F75504	X	X

2019/06/17

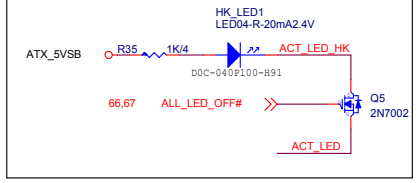
HOTKEY POWER



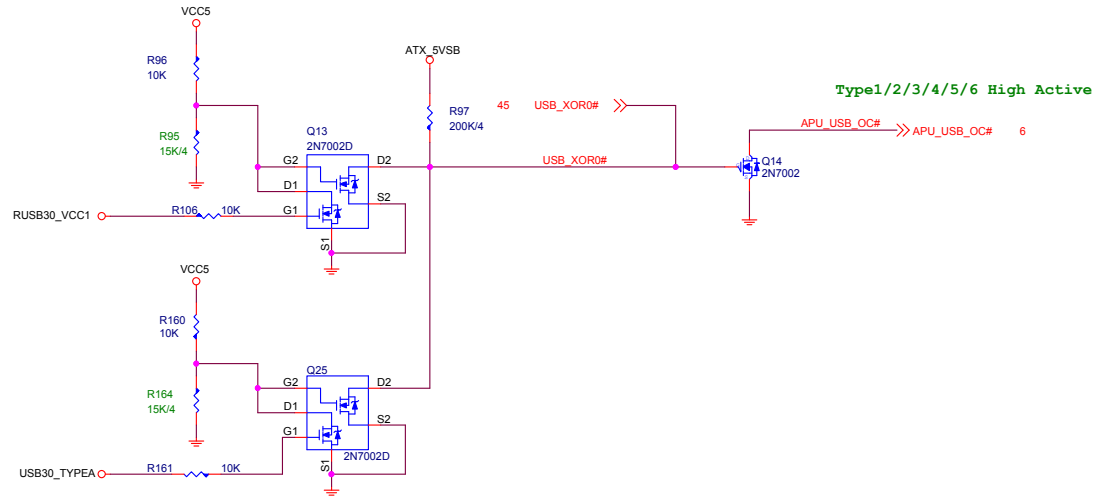
USB Flash BIOS



LED close to USB port

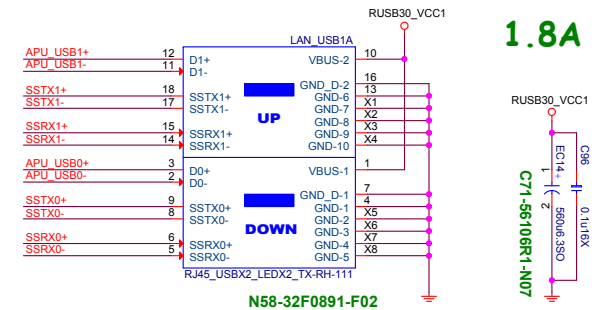
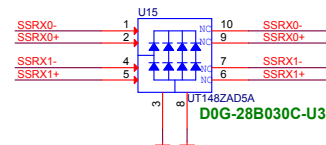
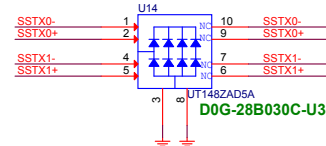
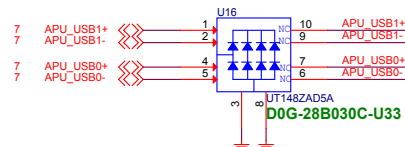


## CPU USB\_OC



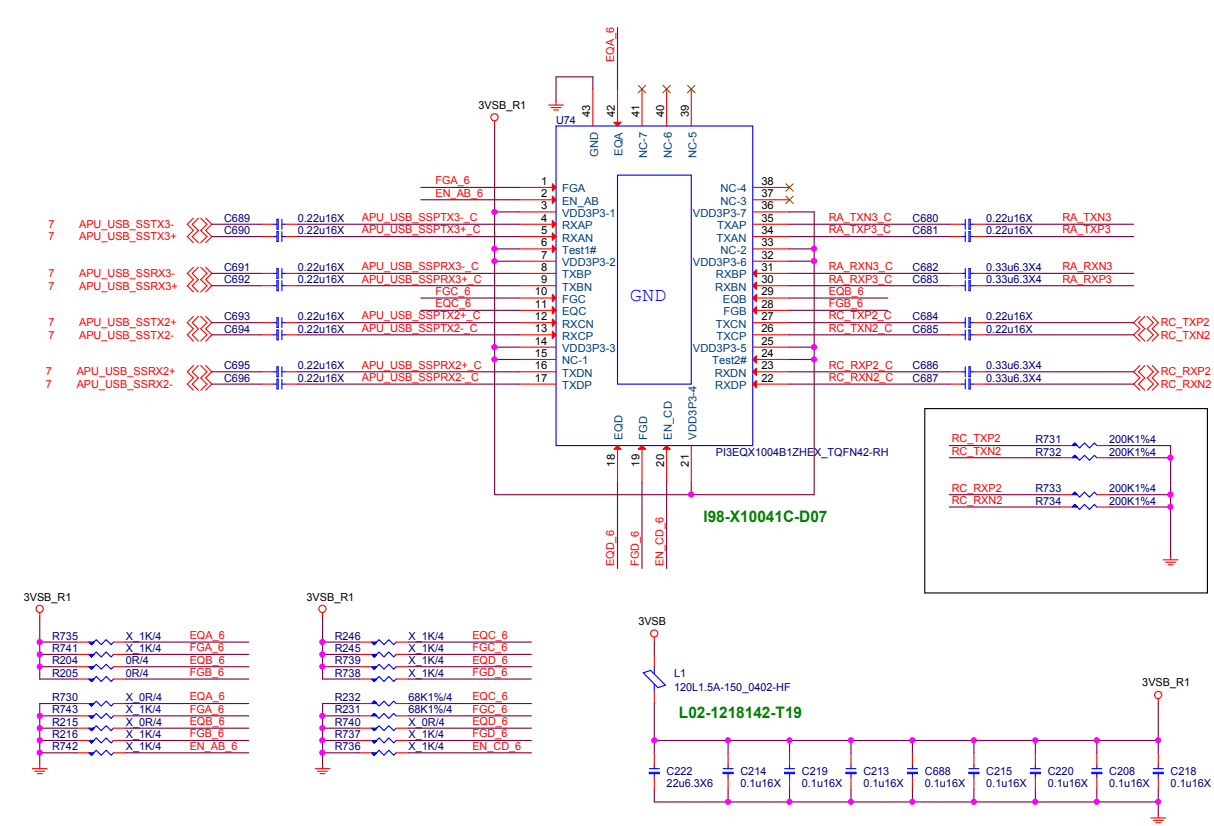
## Rear USB3.1 GEN1 5V@1.8A

7	APU_USB_SSRX1+	C122	0.33u6.3X4	SSRX1+
7	APU_USB_SSRX1-	C123	0.33u6.3X4	SSRX1-
7	APU_USB_SSRX0+	C126	0.33u6.3X4	SSRX0+
7	APU_USB_SSRX0-	C128	0.33u6.3X4	SSRX0-
7	APU_USB_SSTX0+	C108	0.22u16X	SSTX0+
7	APU_USB_SSTX0-	C112	0.22u16X	SSTX0-
7	APU_USB_SSTX1+	C102	0.22u16X	SSTX1+
7	APU_USB_SSTX1-	C104	0.22u16X	SSTX1-



MICRO-STAR INT'L CO.,LTD			
MS-7C91			
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TYPE-A PI3EQX1004 Redriver

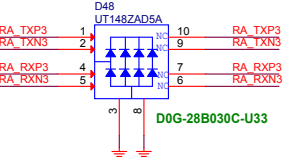
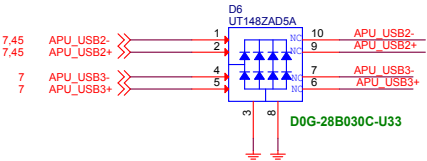
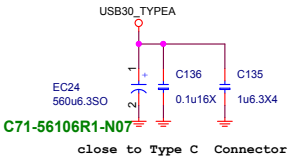


EQ	dB		EQ	FG
0	10.9	0 to GND	USB3_TX4	A
R	6.7	68K to GND	USB3_RX4	B
F	8.9	NC	USB3_TX3	C
1	13.1	0 to VDD	USB3_RX3	D

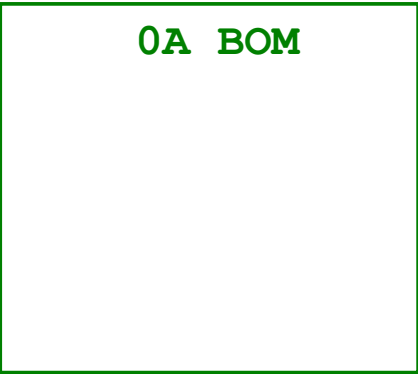
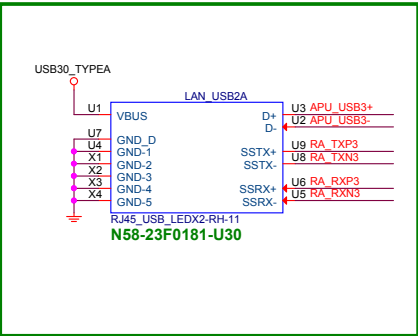
FG	dB		FG	dB	
0	-3	0 to GND	0	-3	0 to GND
R	-1.5	68K to GND	R	-1.5	68K to GND
F	0	NC	F	0	NC
1	2	0 to VDD	1	2	0 to VDD

Rear TYPE-A

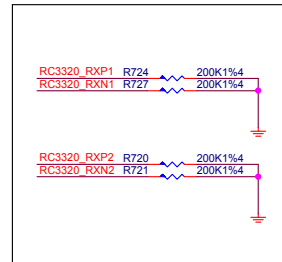
Rear TYPE-C



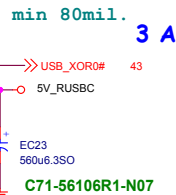
GEN2 0.9A



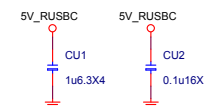
## USB Type-C MUX with Configuration Channel (CC)



## VBUS EN



Current Mode

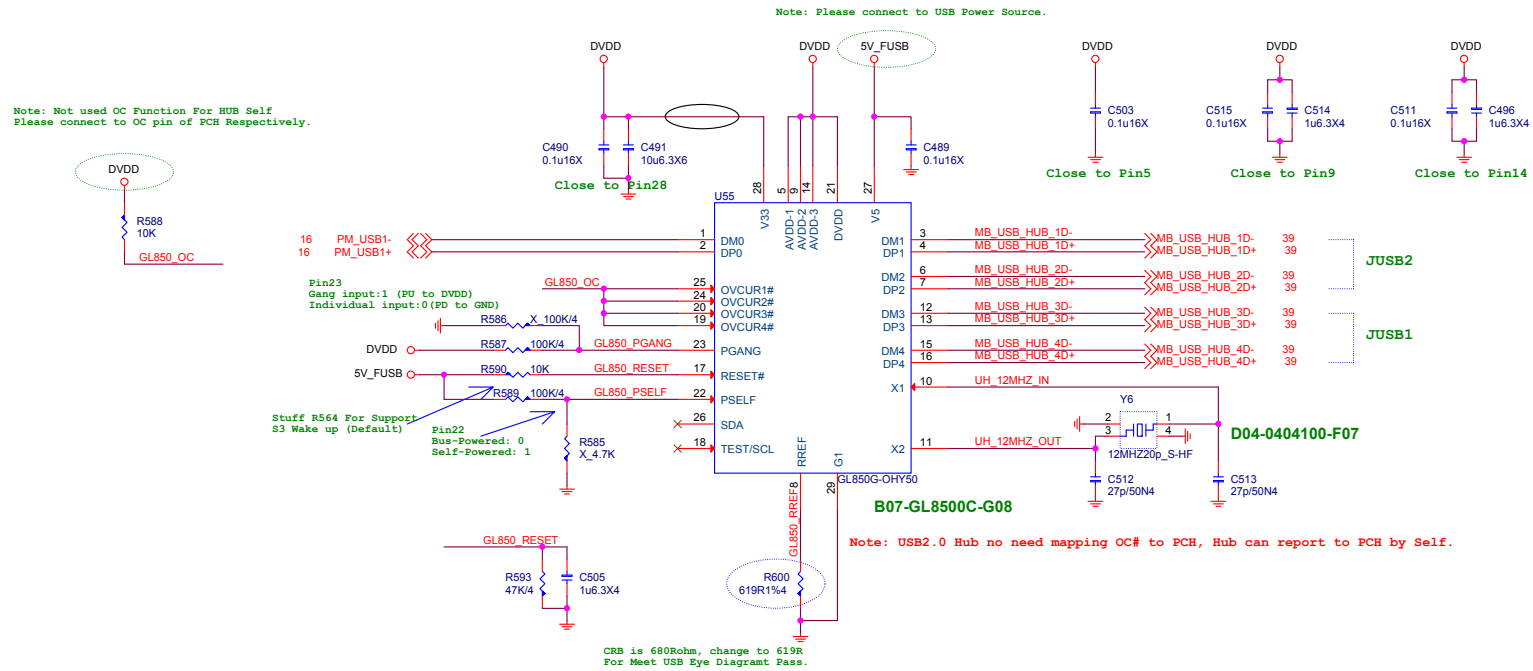


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Size Custom	Document Description <b>Rear USB3.1 Type C / mux</b>	Rev 20
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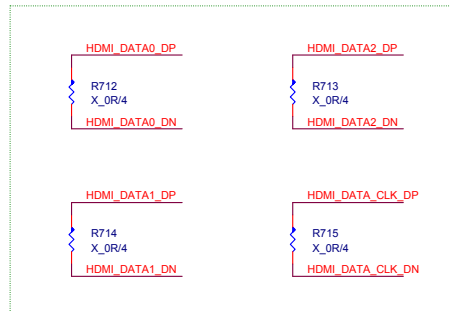
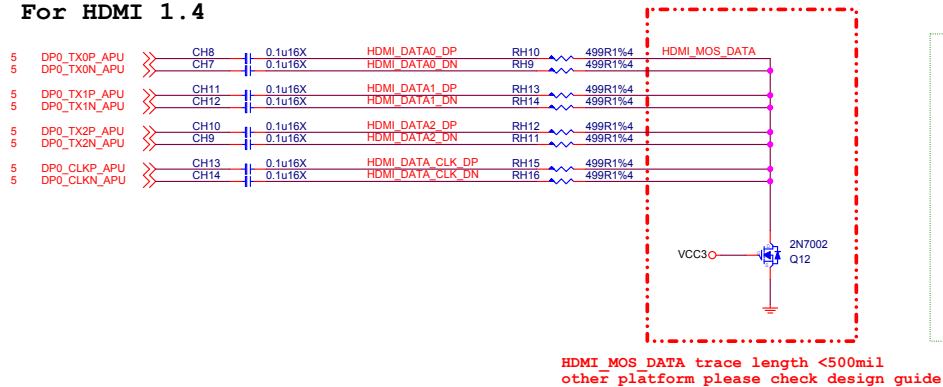
# GL850G USB2.0 HUB

## 5V\_FUSB

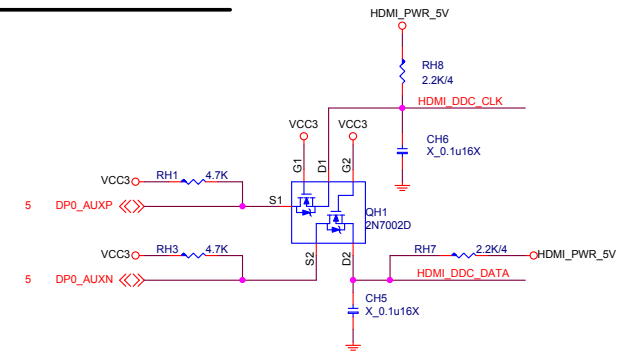


# HDMI CONNECTOR

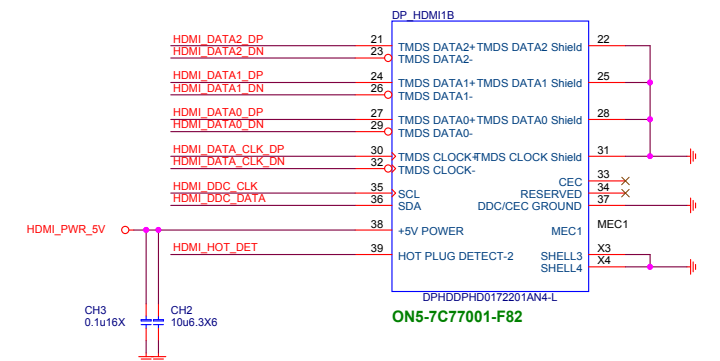
For HDMI 1.4



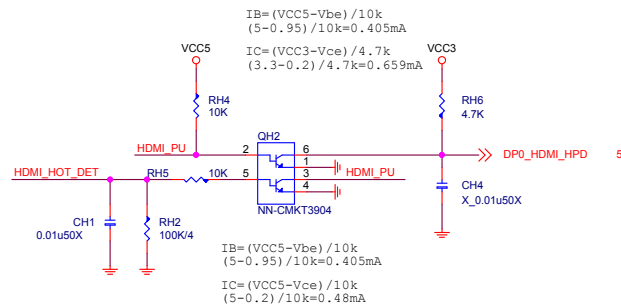
## AUX Level Shifter



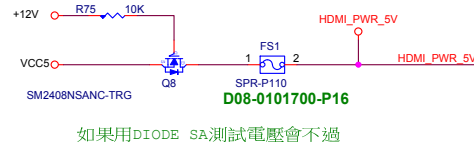
## Connector



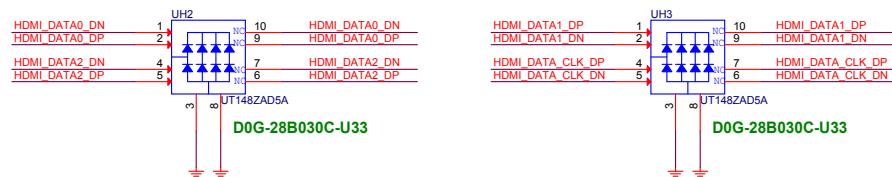
## HPD Circuit



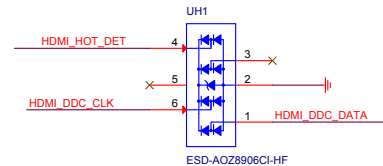
## Connector Power



## For EMI



## 注意:耐壓5v零件

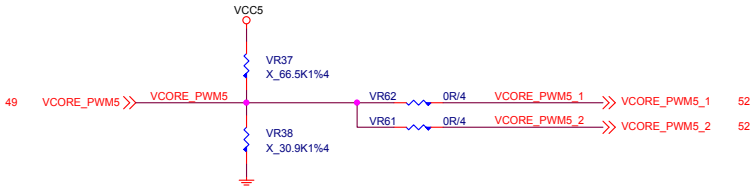
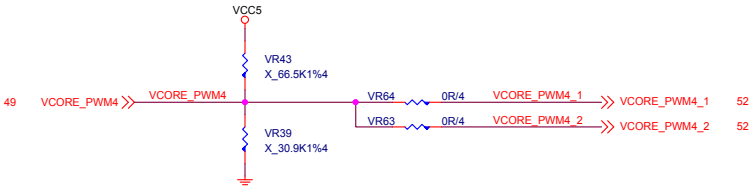
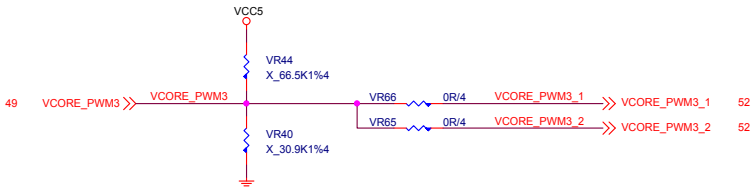
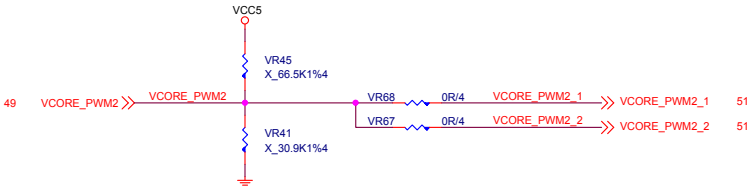
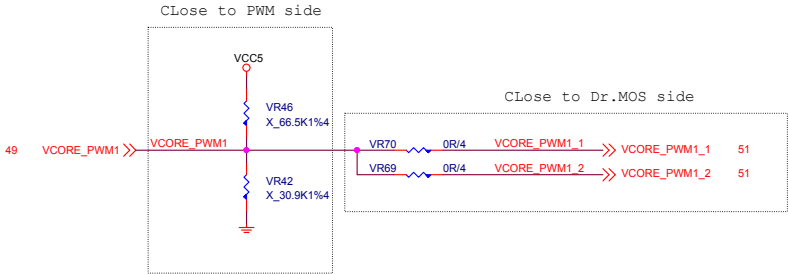




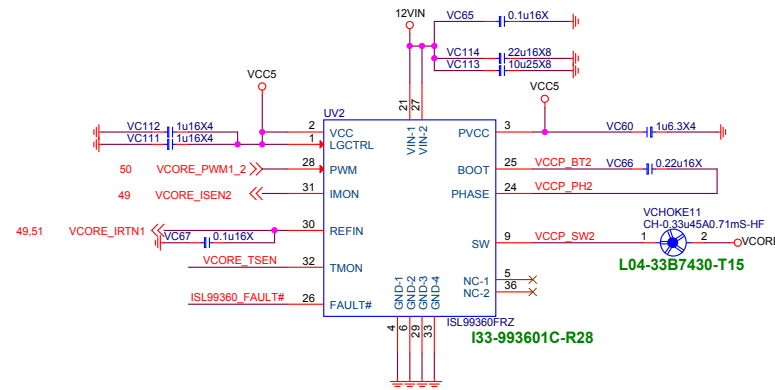
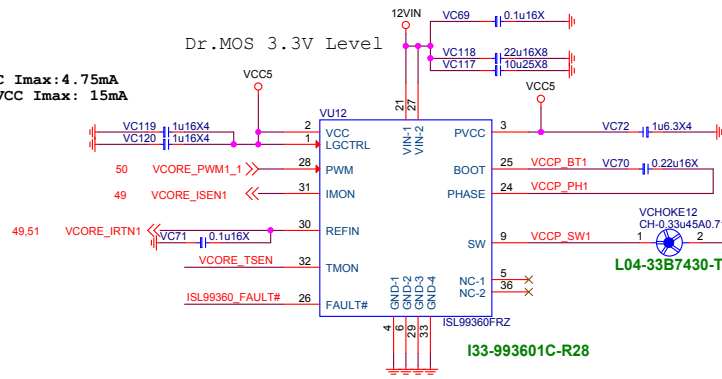




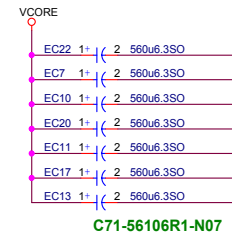
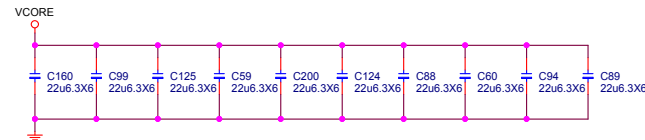
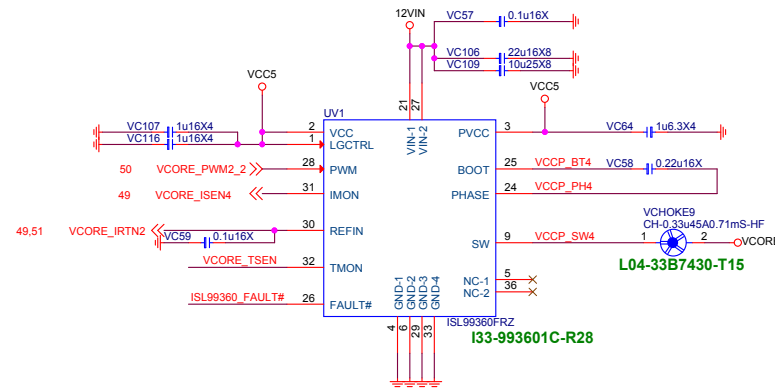
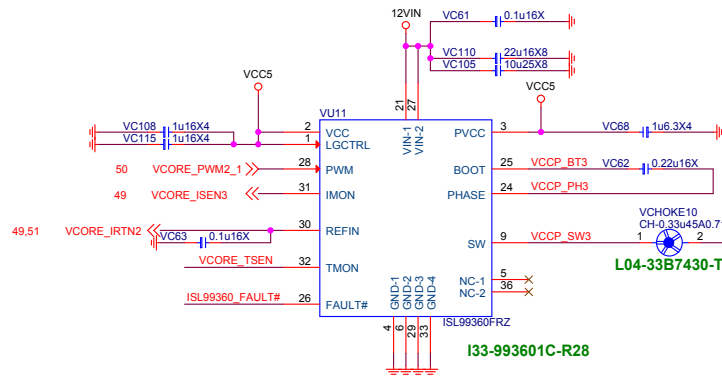
CPU\_CORE Driver IC      VCore Double    10-PHASE



VCC I<sub>max</sub>: 4.75mA  
IPVCC I<sub>max</sub>: 15mA



49,52,53 ISL99360\_FAULT# << ISL99360\_FAULT#  
49,52 VCCORE\_TSEN << VCCORE\_TSEN



C71-56106R1-N07

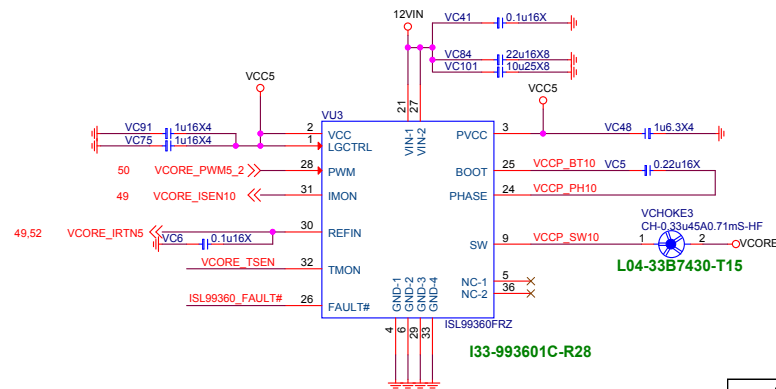
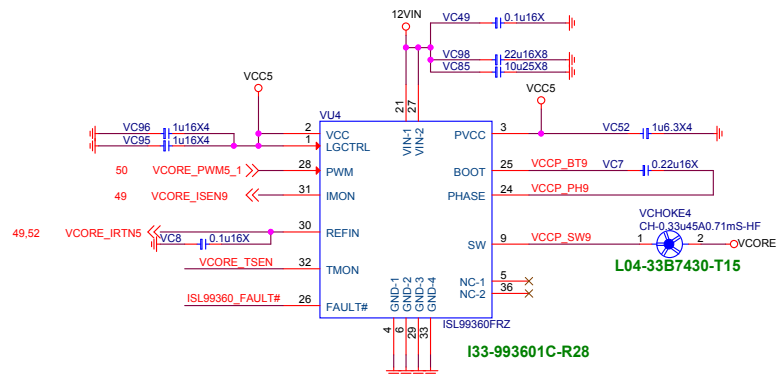
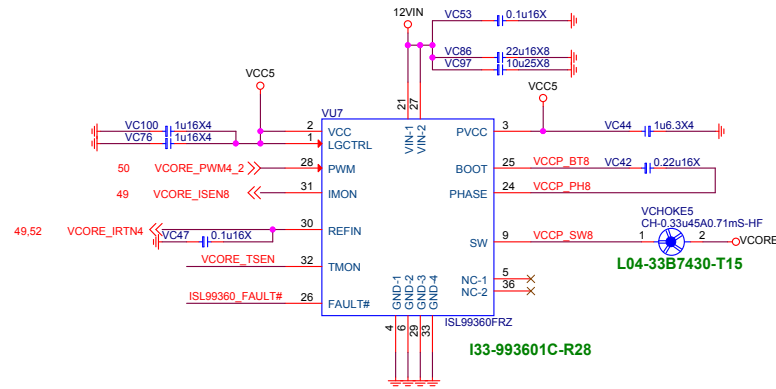
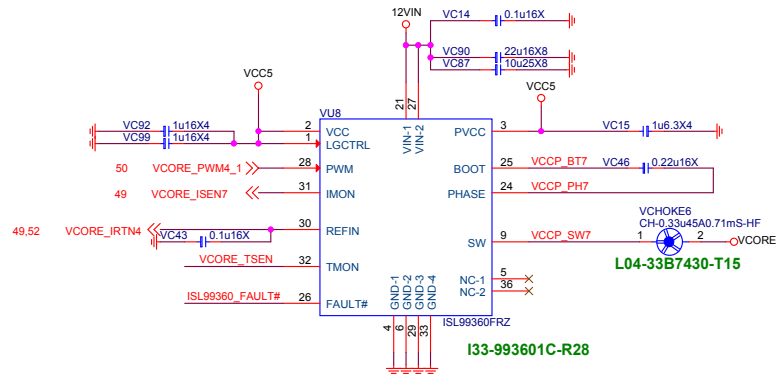
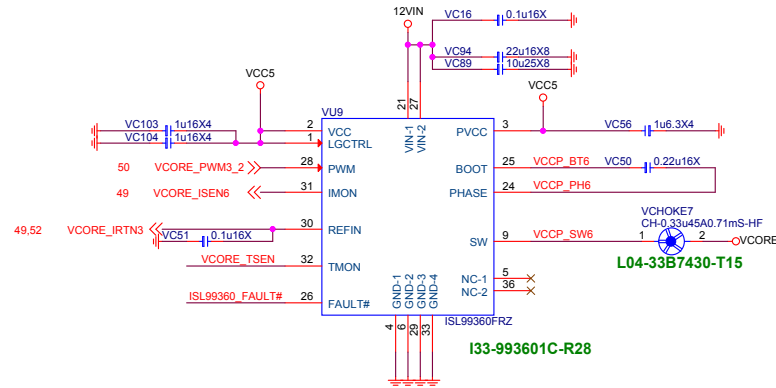
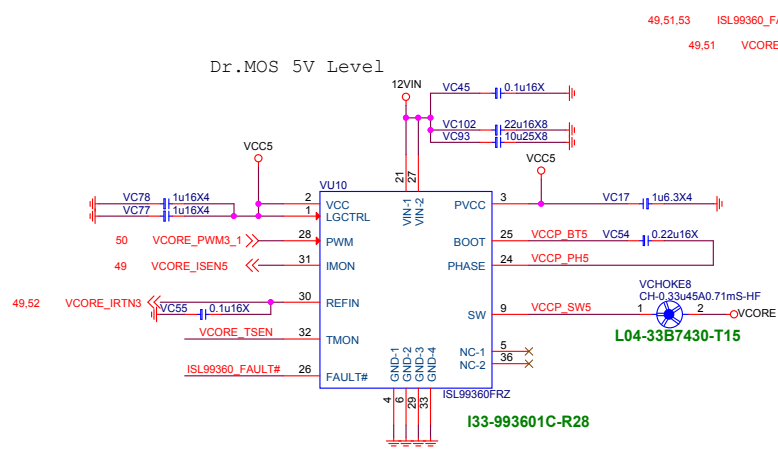


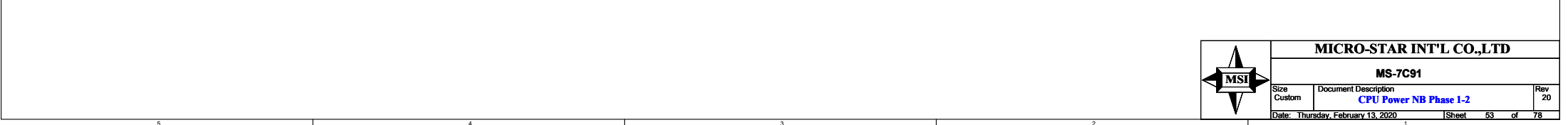
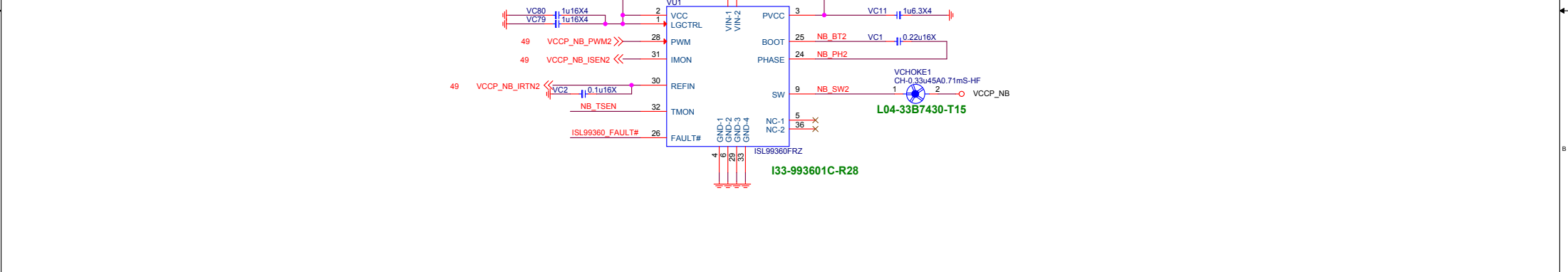
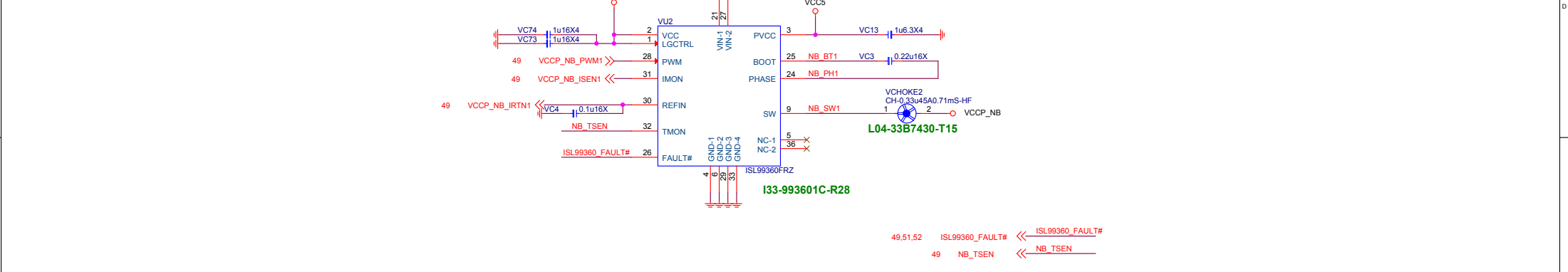
MICRO-STAR INT'L CO.,LTD

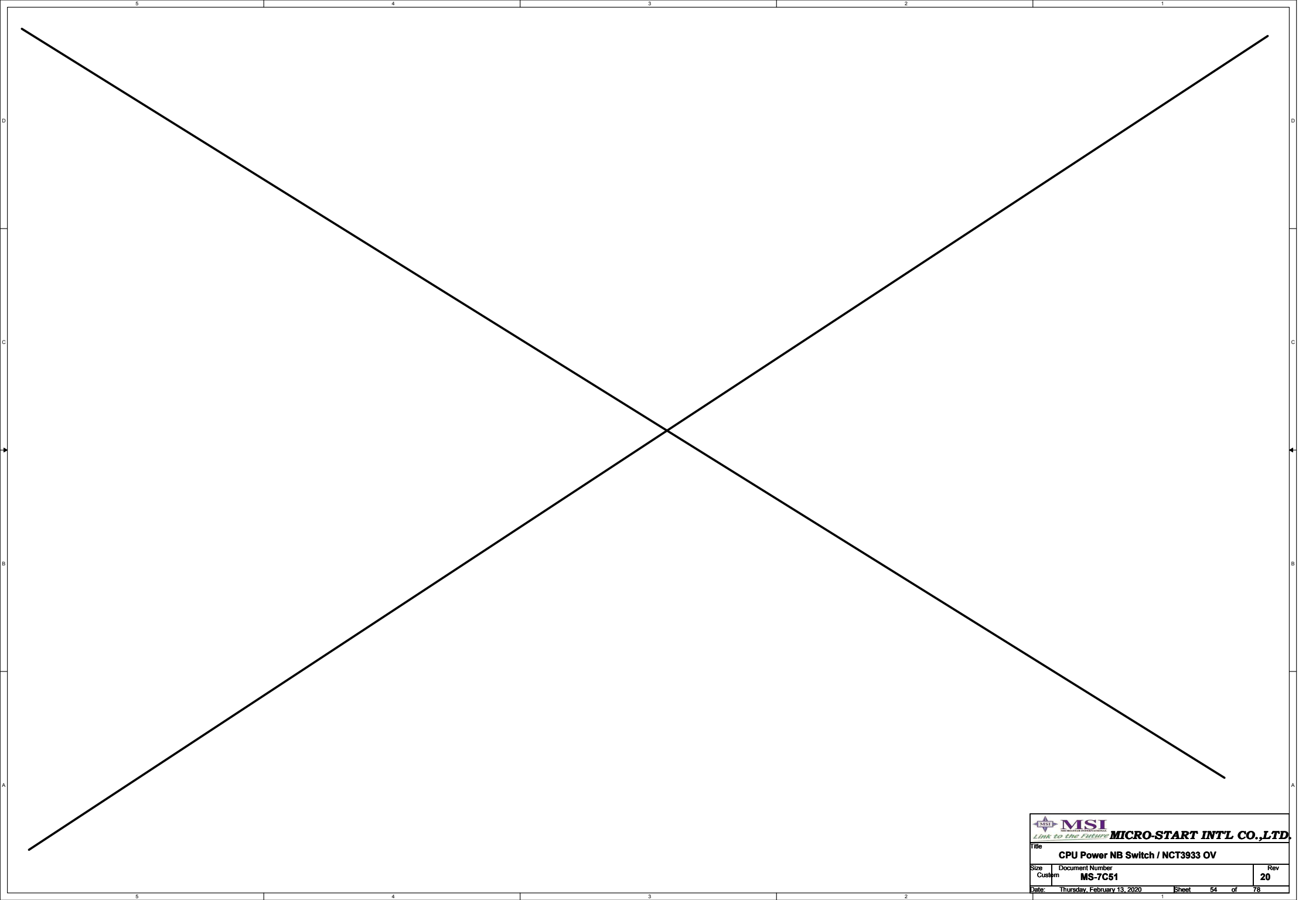
MS-7C91


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Dr.MOS 5V Level







 <b>MSI</b> <small>Micro-Star International</small> <i>Link to the Future</i>			<b>MICRO-START INTL CO.,LTD.</b>		
<b>Title</b> CPU Power NB Switch / NCT3933 OV					
<b>Size</b> Custom	<b>Document Number</b> MS-7C51				<b>Rev</b> 20
<b>Date:</b> Thursday, February 13, 2020	<b>Sheet</b> 54	<b>of</b> 78			

## CPU 1.8V S5

CPU 1.8V\_S5@0.5A  
CPU\_VDDP\_S5@1A  
AUDIO1.8V@0.25A

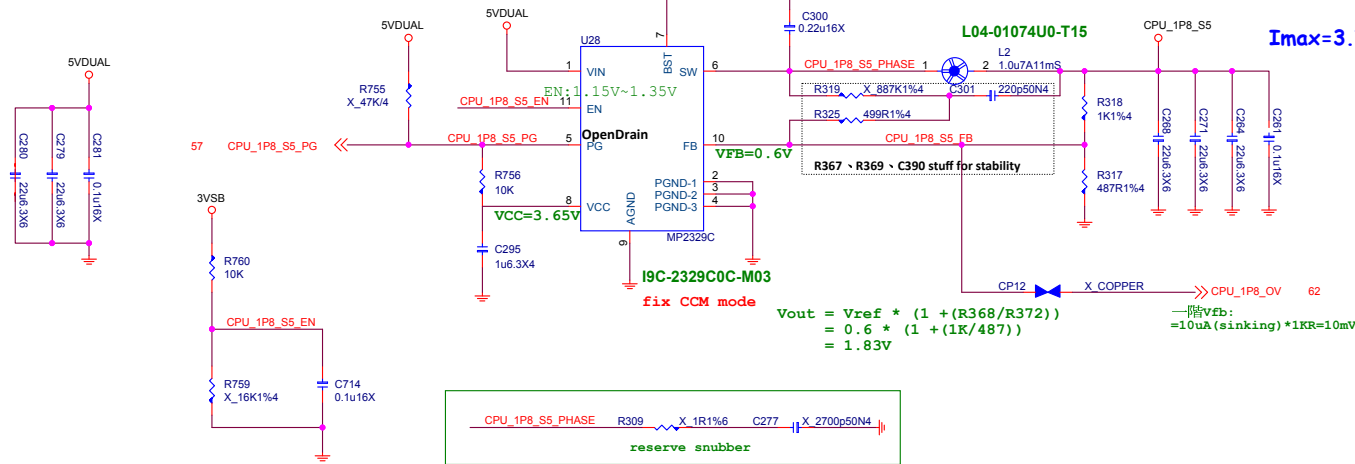
Input Current =  $(6.5A \cdot 1.8V) / 5V / 0.8 = 3A$

Continuous Conduction Mode (CCM)

CPU\_1P8\_BST ~ CPU\_1P8\_BST\_R > 50 mils.

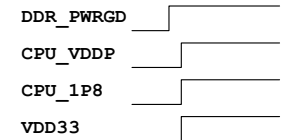
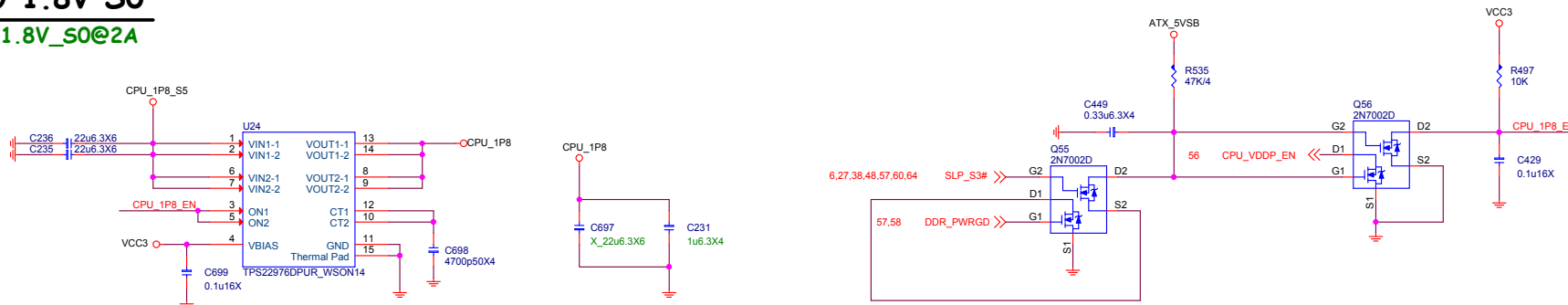
OCP = 6.5A

I<sub>max</sub> = 3.75A(S5+S0)



## CPU 1.8V S0

CPU 1.8V\_S0@2A



MICRO-STAR INT'L CO.,LTD

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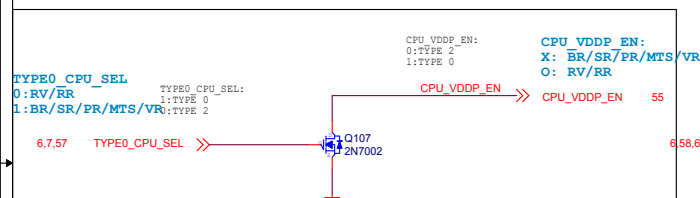
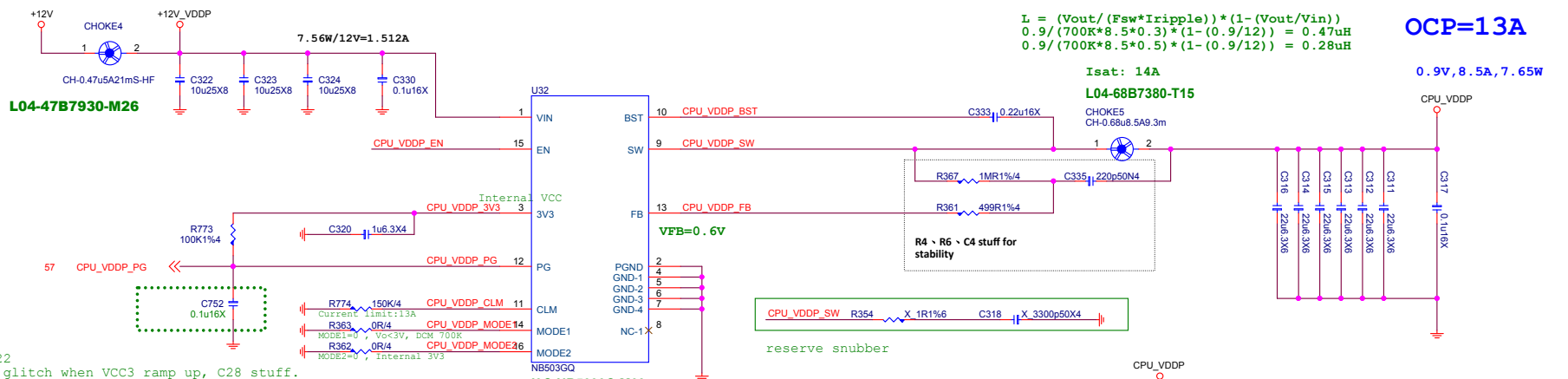
Size	Document Description	Rev
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**0.9V@50:8.5A**

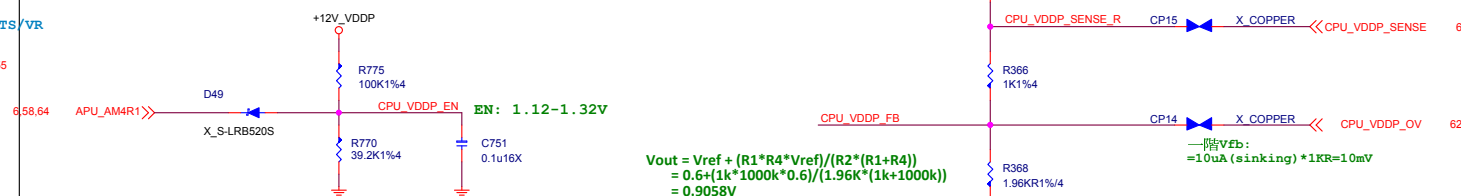
$$L = (V_{out} / (F_{sw} * I_{ripple})) * (1 - (V_{out} / V_{in}))$$
$$0.9 / (700K * 8.5 * 0.3) * (1 - (0.9 / 12)) = 0.47 \mu H$$
$$0.9 / (700K * 8.5 * 0.5) * (1 - (0.9 / 12)) = 0.28 \mu H$$

OCP=13A

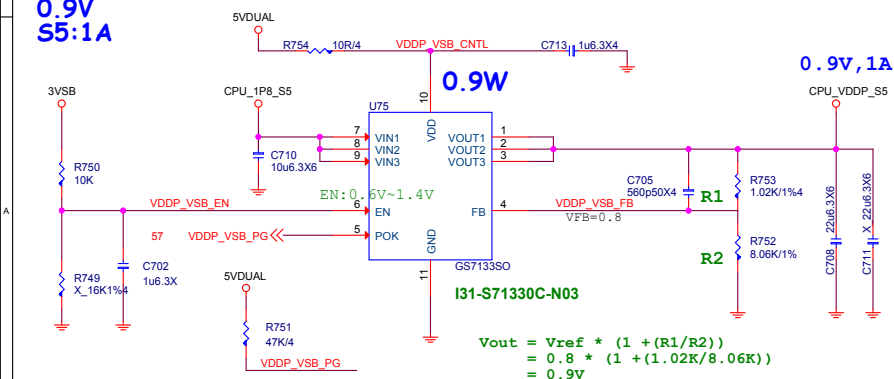
0.9V, 8.5A, 7.65W



CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
BR	0	1	0	SPEC as Support
NA		0	0	0
SR	2	1	CPU VDDP NOT SUPPORT TYPE2	
RV/RR	3/5	0	1	1
MTS/VR	4/6	1	CPU VDDP NOT SUPPORT TYPE4/6	



0.9V  
S5:1A



**MICRO-STAR INT'L CO.,LTD**

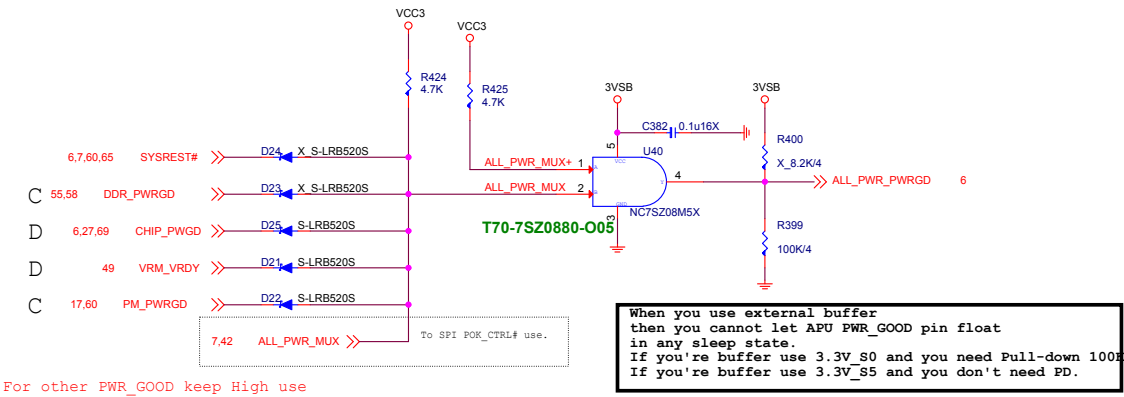
MS-7C91

Size Custom	Document Description <b>CPU Power VDDP - NB503</b>	Rev 20
Date: Thursday, February 13, 2020		Sheet 56 of 78



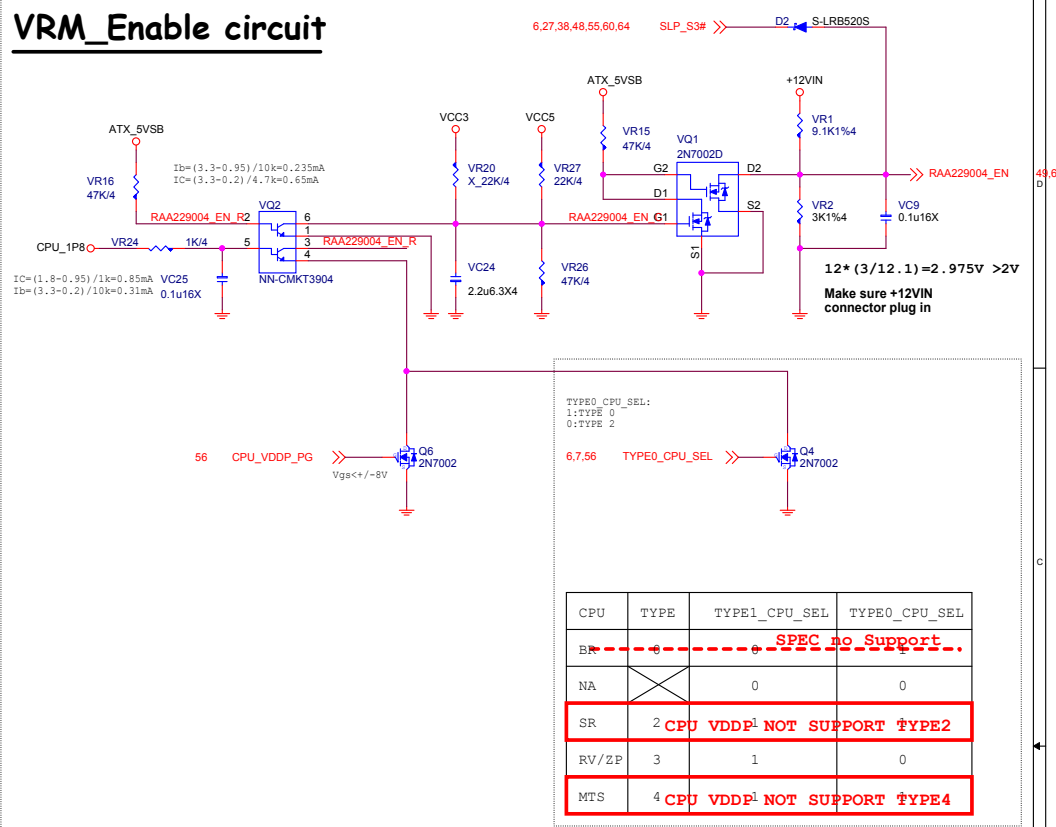
ALL POWER GOOD MUX

S0 PG



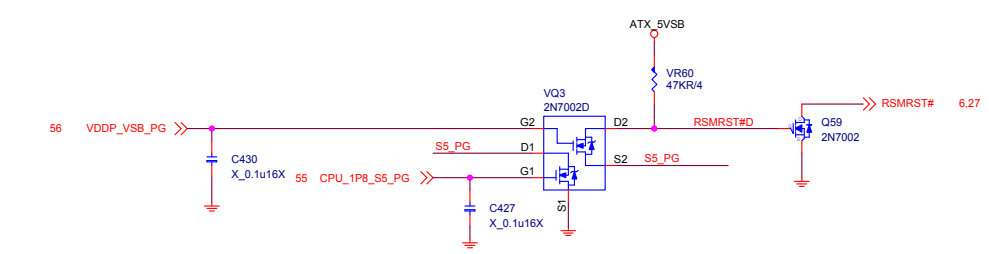
For other PWR\_GOOD keep High use

VRM\_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	0
NA	1	0	0
SR	2	1	0
RV/ZP	3	1	0
MTS	4	1	0

S5 PG



DDR4\_1.2V@28.7A

18A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

$$\begin{aligned} \text{Rocset} &= 1.5 * \text{Imax} * \text{Rdson}(\text{Low side}) / \text{Iocset} \\ &= 1.5 * 28.7\text{A} * 2\text{mohm} / 10\text{uA} \\ &= 8.61\text{K} \end{aligned}$$

OCP = 43.05A; Choke Isat=43A

$$\begin{aligned} \text{Rocset} &= 1.5 * \text{Imax} * \text{Rdson}(\text{low}) / \text{Iocset} \\ \text{R639} &= 1.5 * 28.7 * 2\text{mohm} / 10\text{uA} \\ \text{R639} &= 8.61\text{K} \end{aligned}$$

Rdson(Low Side) 5V

D03-4C02403-O05:3.3 ~ 4mohm

$$\begin{aligned} 10\text{mV} * (1.96\text{K} / 2.96\text{K}) &= 6.62\text{mV} \\ \text{REFIN}(\text{R625}) &= 6.62\text{mV} / 10\text{uA} = 662\text{R} \end{aligned}$$

DDR VR EN  
FROM SIO\_VDDQ\_EN:R230/R220 stuff  
FROM VPP\_VR\_PG:R230/R220 un stuff

Default:FCCM  
4.5V:FCCM  
2.37V:DEM

Default:FCCM  
L:FCCM  
H:DEM

$$\begin{aligned} \text{Rocset} &= 1.5 * \text{Imax} * \text{Rdson}(\text{Low side}) / \text{Iocset} \\ &= 1.5 * 28.7\text{A} * 2\text{mohm} / 10\text{uA} \\ &= 8.61\text{K} \end{aligned}$$

$$\text{Input Current} = (28.7 * 1.2) / 5 / 0.8 = 8.61\text{A}$$

L04-68B7350-T15

CH0-0.68u15A5mS

C71-56106R1-N07

OL4-7C94001-T15

CH0-0.47u36A0.88m

C71-56106R1-N07

C71-56106R1-N07

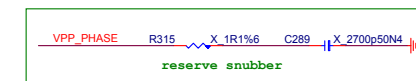


MICRO-STAR INT'L CO.,LTD

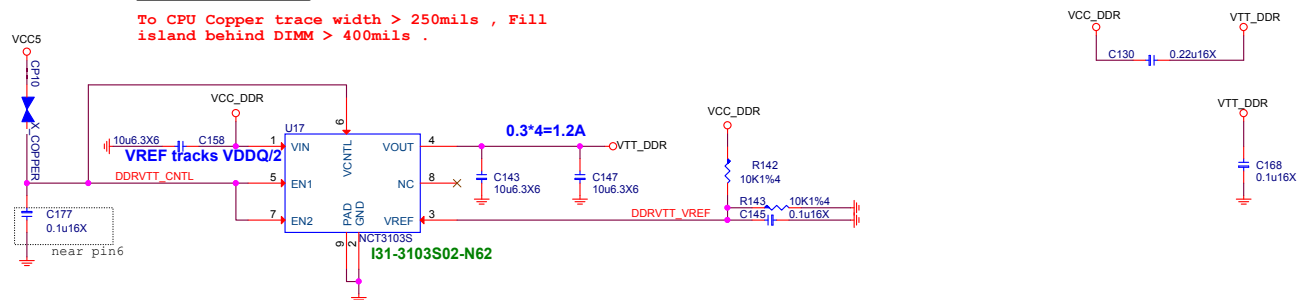
MS-7C91

Size	Document Description	Rev
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## 2.5V@2.24A



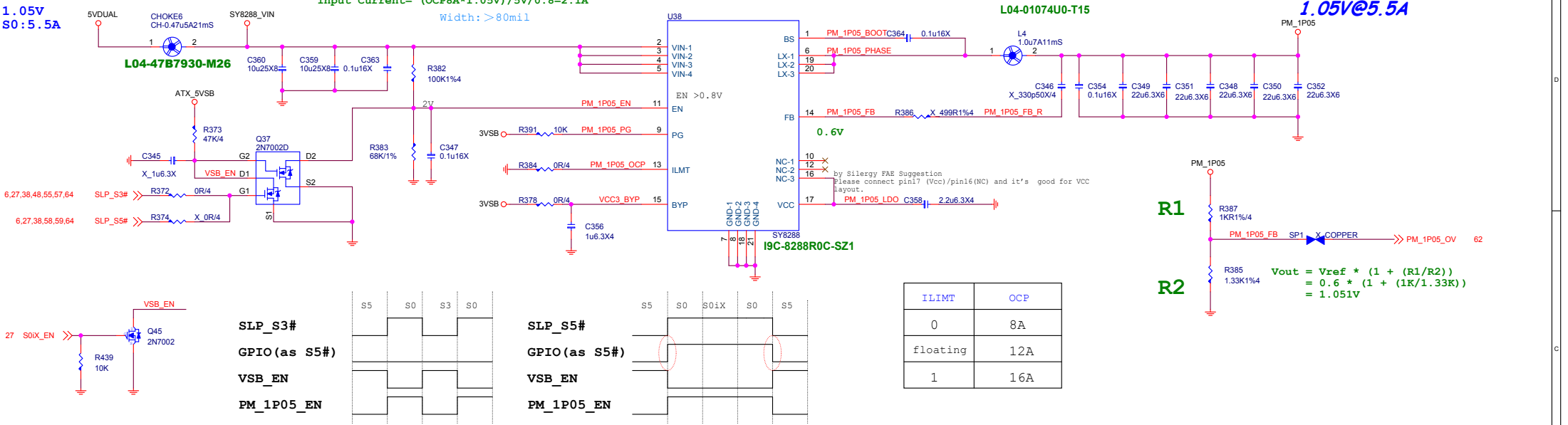
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



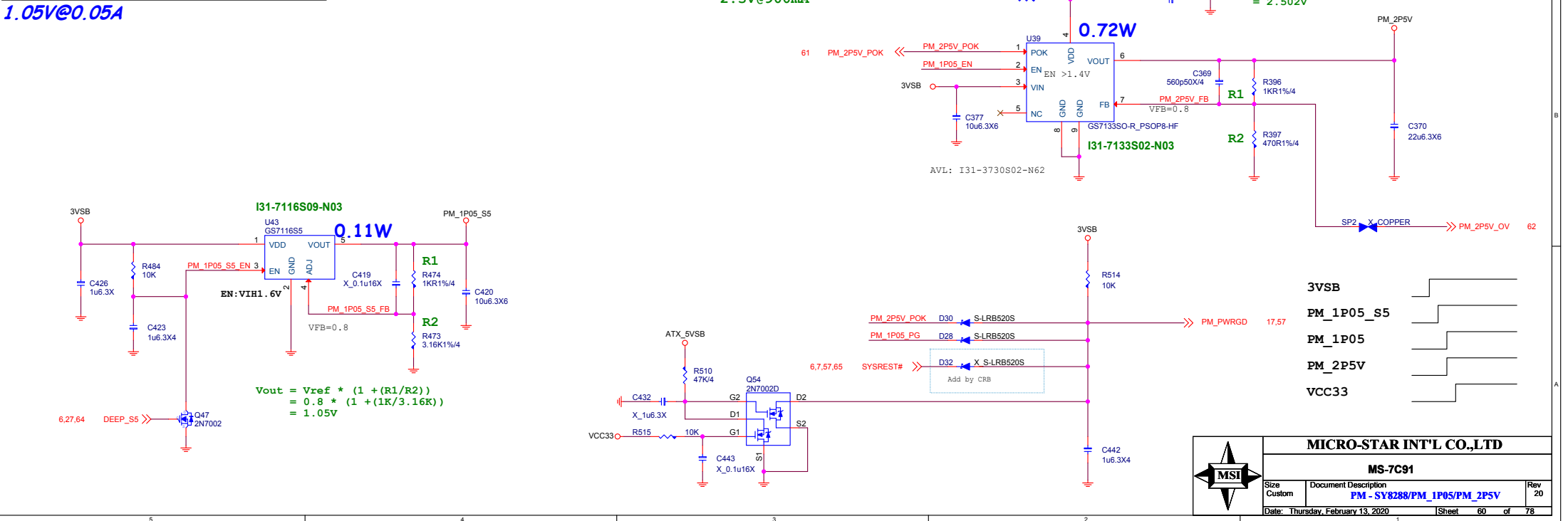
MS-7C91

Size Custom	Document Description <b>DDR VPP25 / VTT</b>	Rev 20
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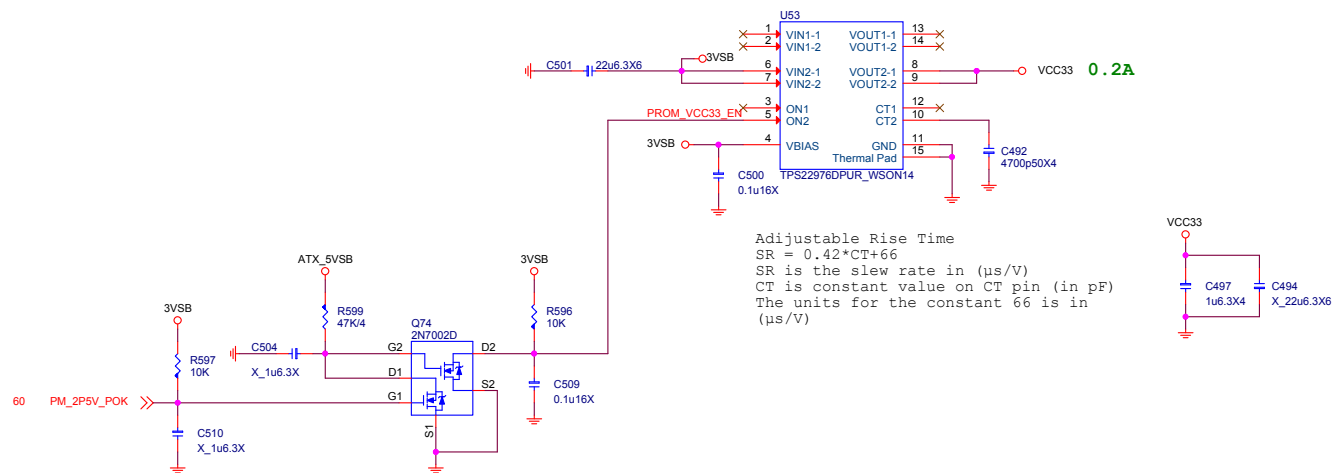
FOR Promontory 1.05V\_S0



FOR PROM PM\_1P05\_S5



## VCC33@0.2A



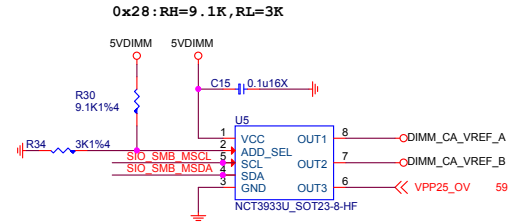
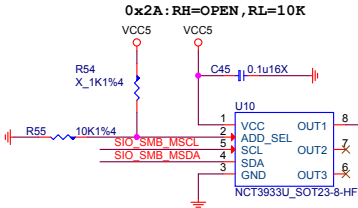
MS-7C91

Size Custom	Document Description <b>PM - XXXXXXXX</b>	Rev 20
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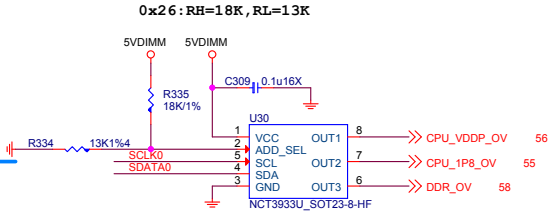
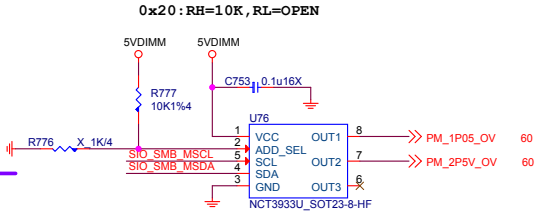
Over Voltage Control IC

UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



6,27,49 SIO\_SMB\_MSCL >>> SIO\_SMB\_MSCL  
6,27,49 SIO\_SMB\_MSDA >>> SIO\_SMB\_MSDA



6,11 SCLK0 >>> SCLK0  
6,11 SDATA0 >>> SDATA0

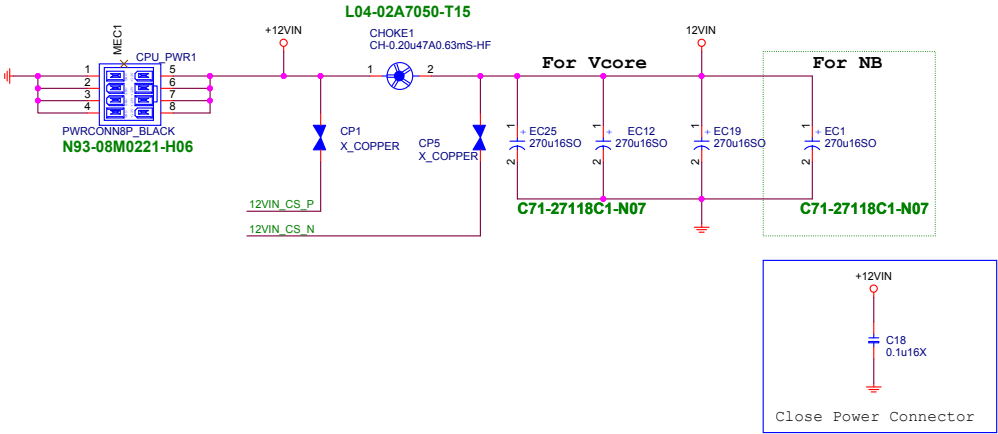


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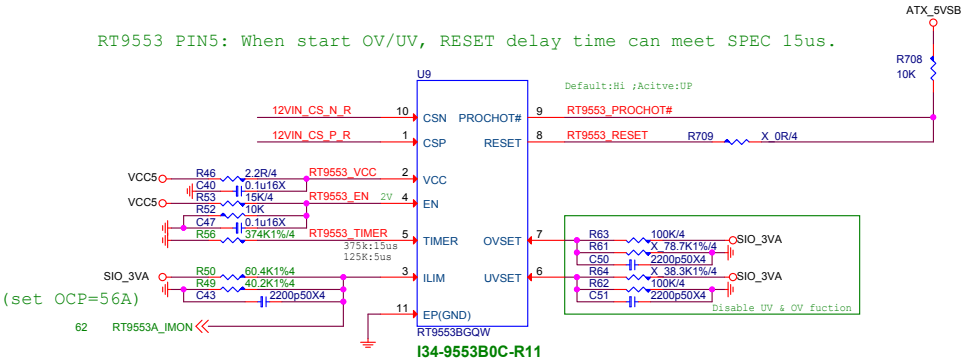
MS-7C91

Size Custom	Document Description OV Control - NCT3933	Rev 20
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CPU POWER CONNECTOR



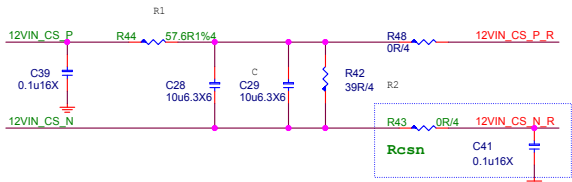
RT9553B CURRENT SENSE



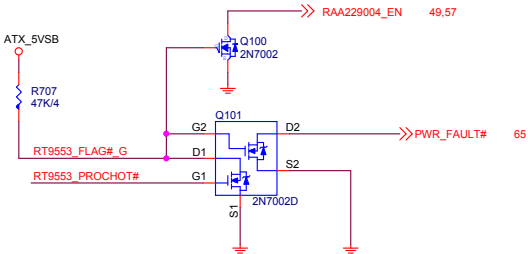
$$\Delta V_{ILIM} = 10\mu A * [ (60.4K * 40.2K) / (60.4K + 40.2K) ]$$
$$= 226mV$$

$$I_{sense} = V_{ILIM} / 100 * R_{sense}$$

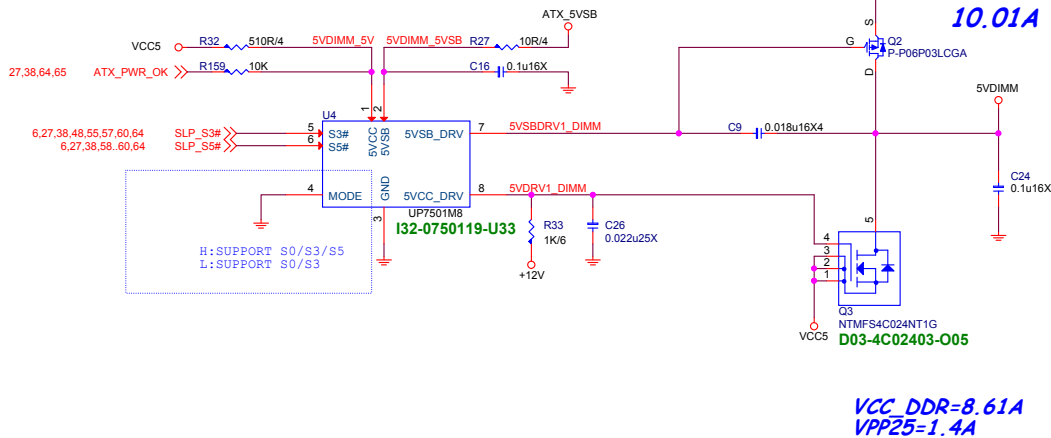
$$\Delta I_{sense} = 226mV / 100 * 0.39m = 5.795A$$



Vcore		SOC	
D=Vout/Vin		D=Vout/Vin	
Vin = 12	> input voltage	Vin = 12	> input voltage
Vout = 2	> output Vcore	Vout = 1.55	> output Vcore
D = 0.166667		D = 0.129167	
Io = Icore(max)*0.8		Io = Icore(max)*0.8	
I core(max) = 200	> Vcore current	I core(max) = 75	> Vcore current
I avg. = 160	A	I avg. = 60	A
I ripple={ Io*√D*√(1-D) } / Phase		I ripple={ Io*√D*√(1-D) } / Phase	
Phase = 10	phase	Phase = 2	phase
I ripple = 5.962848	A	I ripple = 10.06153	A
How many pcs. Of Cap.		How many pcs. Of Cap.	
I ripple(cap) = 4700	m A	I ripple(cap) = 4700	m A
COETEMP = 1		COETEMP = 1	
Input Cap. = 2	pcs.	Input Cap. = 3	pcs.



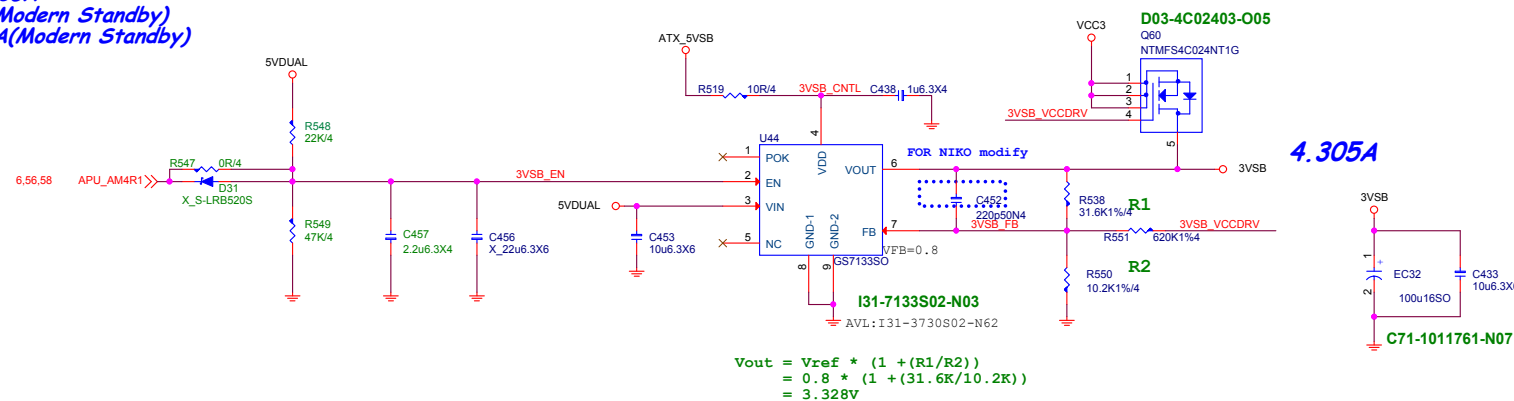
## 5VDIMM FOR DDR



## 3VSB cost down

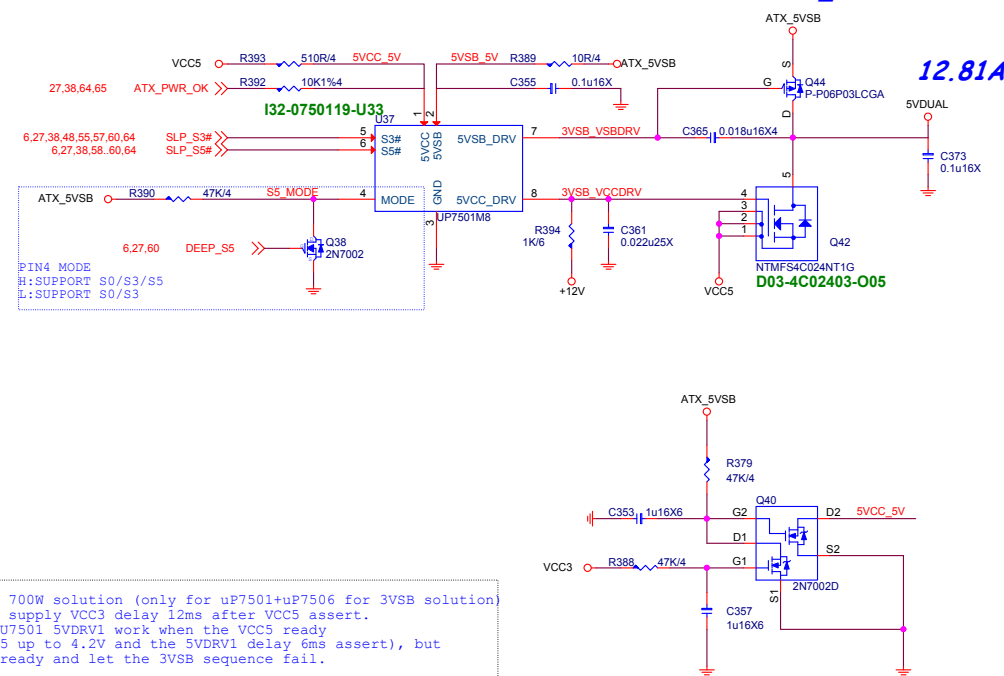
3.3V@4.305A

```
CPU:VDD_33_S5=0.25A
CHIP:VDD_33_S5=0.07A
PCIE=(375mA*5)=1.875A
M.2WIFI= 0.78A
RT8111H LAN=0.18A
PM_1P05_S5 : 0.05A
PM_2P5V : 0.9A(Modern Standby)
PCH VCC33 : 0.2A(Modern Standby)
```



### 5VDUAL For 3VSB/CPU1.8V/VDDP

LDOVDD=93.6mA  
CPU\_1P8\_S5 VIN=3A  
PM\_1P05 VIN=2.1A  
3VSB = 4.71A  
LED\_VCC5 = 3A



For power 700W solution (only for uP7501+uP7506 for 3VSB solution  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip uP7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but  
VCC3 not ready and let the 3VSB sequence fail.



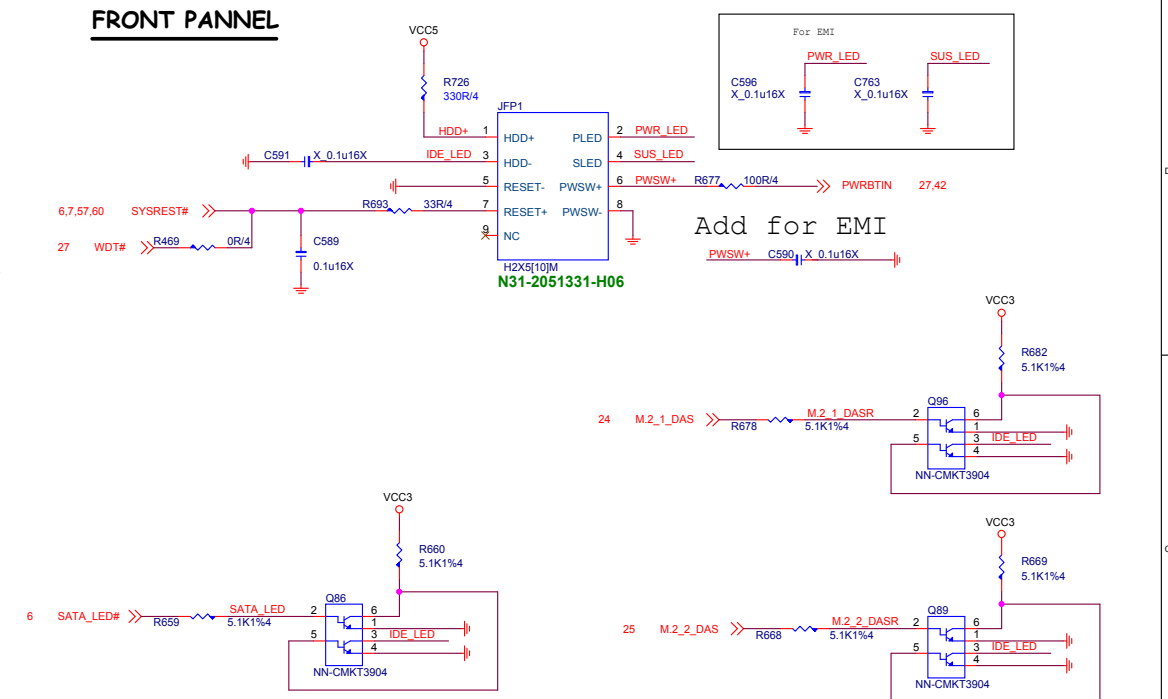
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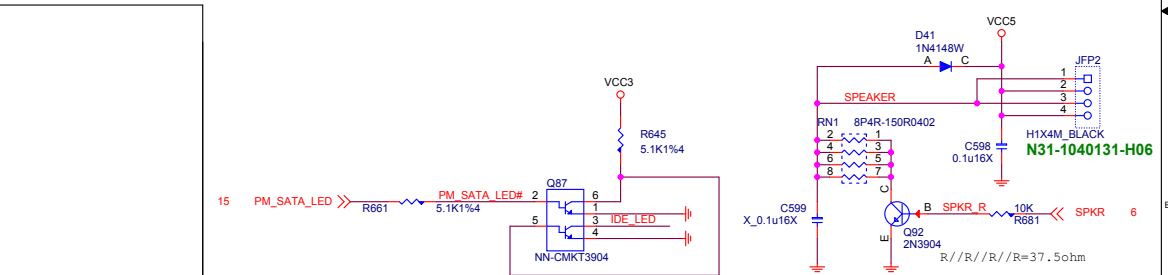
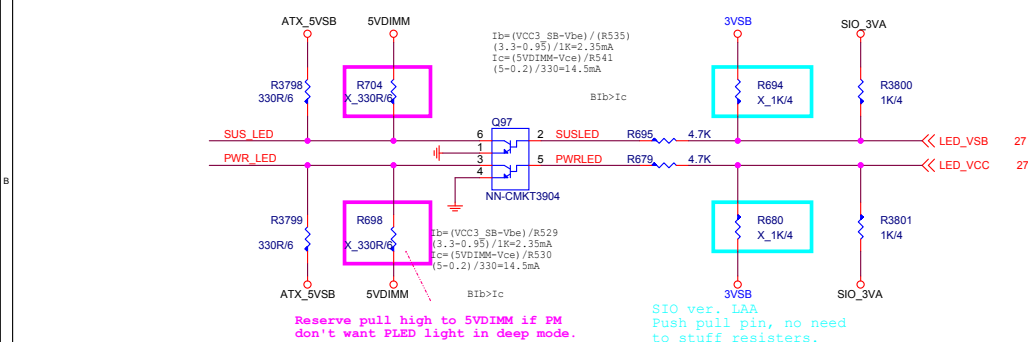
Size Custom	Document Description <b>ACPI - 5VDIMM / 3VSB</b>	Rev 20
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## FRONT PANNEL



### Voltage Mearsure Point



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### EZ Debug LED

The diagram illustrates the EZ Debug LED system, showing four main sections: CPU, DRAM, VGA, and DEVICE. Each section includes a schematic diagram and a table for GPIO pin configurations.

#### CPU

**Schematic:** The CPU section shows a circuit for CPU\_LED1 (LED04-R-20mA2.4V) connected to VCC5 through resistor R117 (1K/4). The LED is connected to the collector of transistor Q17 (2N7002), which is controlled by GPIO44\_CPU (pin 27) through resistor R133 (4.7K). The emitter of Q17 is connected to ground. A second transistor Q15 (2N7002) is connected to VCC3 through resistor R115 (X\_0R/4) and controlled by EGPI096\_DRAM (pin 6,66). The emitter of Q15 is connected to ground.

LED	GPIO	EGPI096	GPIO45	GPIO47
亮	OPEN-Drain	GPO LOW	GPO LOW	GPO LOW
滅	GPO LOW	GPO HIGH	OPEN-Drain	OPEN-Drain

#### DRAM

**Schematic:** The DRAM section shows a circuit for DRAM\_LED1 (LED04-R-20mA2.4V) connected to VCC5 through resistor R122 (1K/4). The LED is connected to the collector of transistor Q19 (2N7002), which is controlled by GPIO45\_VGA (pin 27) through resistor R131 (4.7K). The emitter of Q19 is connected to ground. A second transistor Q15 (2N7002) is connected to VCC3 through resistor R115 (X\_0R/4) and controlled by EGPI096\_DRAM (pin 6,66). The emitter of Q15 is connected to ground.

#### VGA

**Schematic:** The VGA section shows a circuit for VGA\_LED1 (LED04-R-20mA2.4V) connected to VCC5 through resistor R127 (1K/4). The LED is connected to the collector of transistor Q22 (2N7002), which is controlled by GPIO47\_DEVICE (pin 27) through resistor R137 (X\_100K/4). The emitter of Q22 is connected to ground. A second transistor Q15 (2N7002) is connected to VCC3 through resistor R115 (X\_0R/4) and controlled by EGPI096\_DRAM (pin 6,66). The emitter of Q15 is connected to ground.

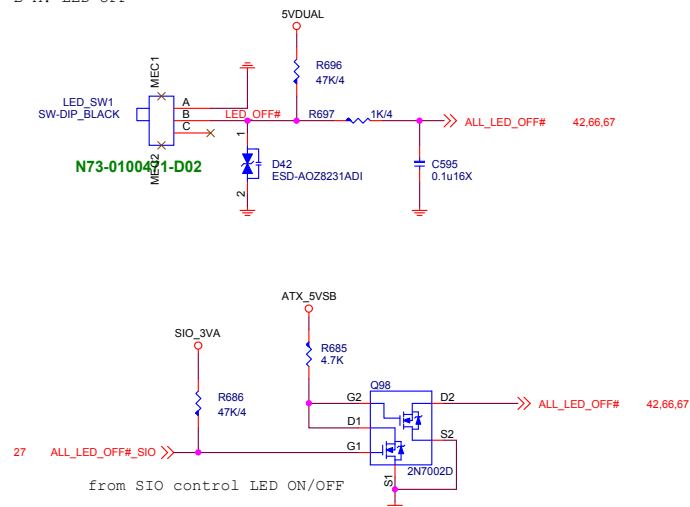
#### DEVICE

**Schematic:** The DEVICE section shows a circuit for BOOT\_LED1 (LED04-R-20mA2.4V) connected to VCC5 through resistor R134 (1K/4). The LED is connected to the collector of transistor Q23 (2N7002), which is controlled by GPIO47\_DEVICE (pin 27) through resistor R137 (X\_100K/4). The emitter of Q23 is connected to ground. A second transistor Q15 (2N7002) is connected to VCC3 through resistor R115 (X\_0R/4) and controlled by EGPI096\_DRAM (pin 6,66). The emitter of Q15 is connected to ground.

LEDGPIO	GPIO44	EGPIO96	GPIO45	GPIO47	default Input
亮	OPEN-Drain	GPO LOW	GPO LOW	GPO LOW	
滅	GPO LOW	GPO HIGH	OPEN-Drain	OPEN-Drain	

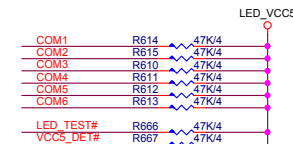
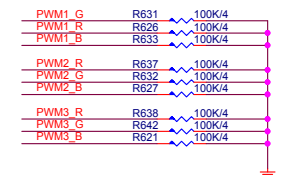
D0C-040P100-H91/D0C-040S500-E07

```
B-C: LED ON(default)
B-A: LED OFF
```



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If you use ADC function, need to separate VREF from AVDD and 4 09VREF stuff for VREF.

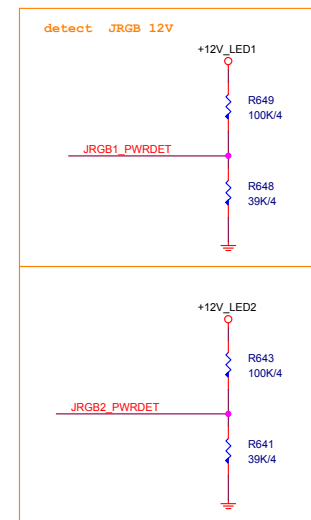
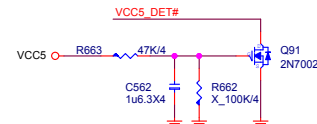


COM1-8 for PWM3  
According to demand configuration.  
Can configuration COM1-8,  
To achieve 8 group Non-synchronized  
onboard LED control.

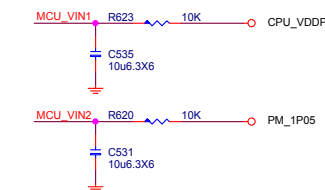
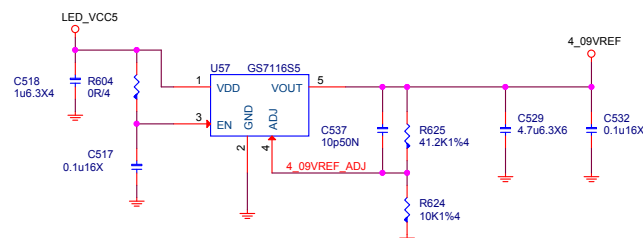
COM9-13 for PWM2  
According to demand configuration.  
If SPEC. don't have JRG82,  
Can configuration COM9-13,  
To achieve 5 group Non-synchronized  
onboard LED control.

PS. COM1 is the first action block,  
next is COM2, and so on.

Pin15,16 can configure to master  
smbus if spec requirement.



Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

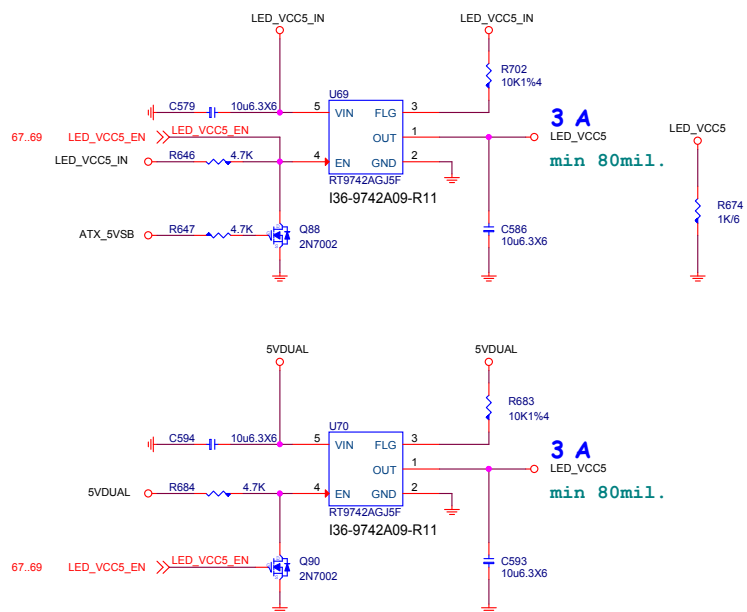


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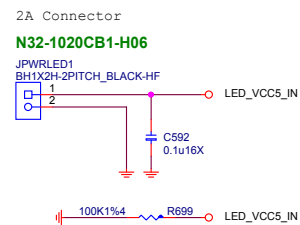
MS-7C91

Size Custom	Document Description <b>MCU - LED Control</b>	Rev 20
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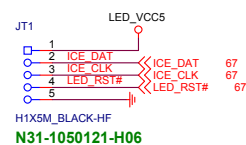
## EXTERNAL POWER INPUT



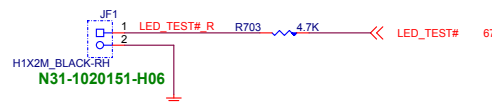
## External Power



## JT1 for FW update



## JF1 for Factory test

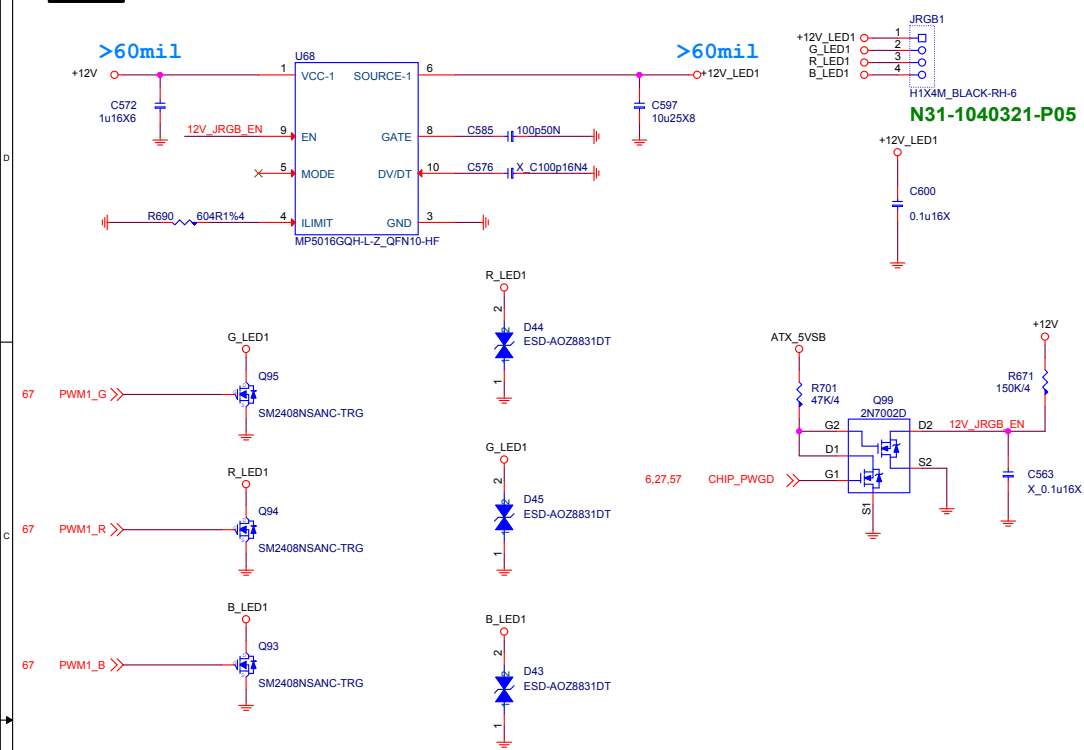
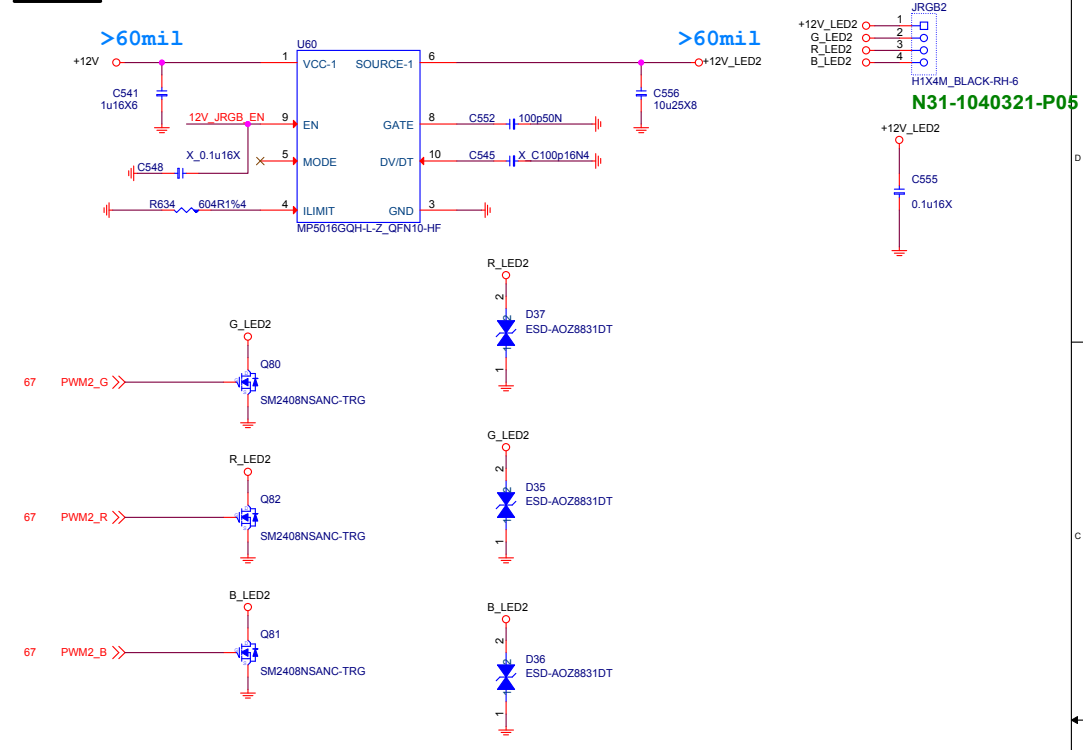
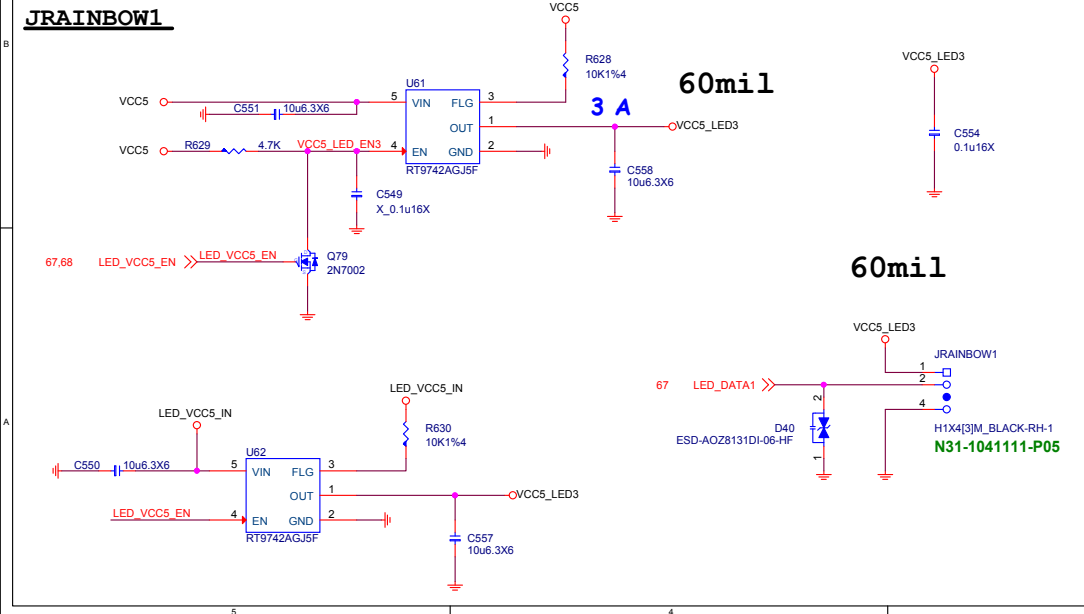
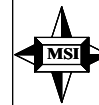
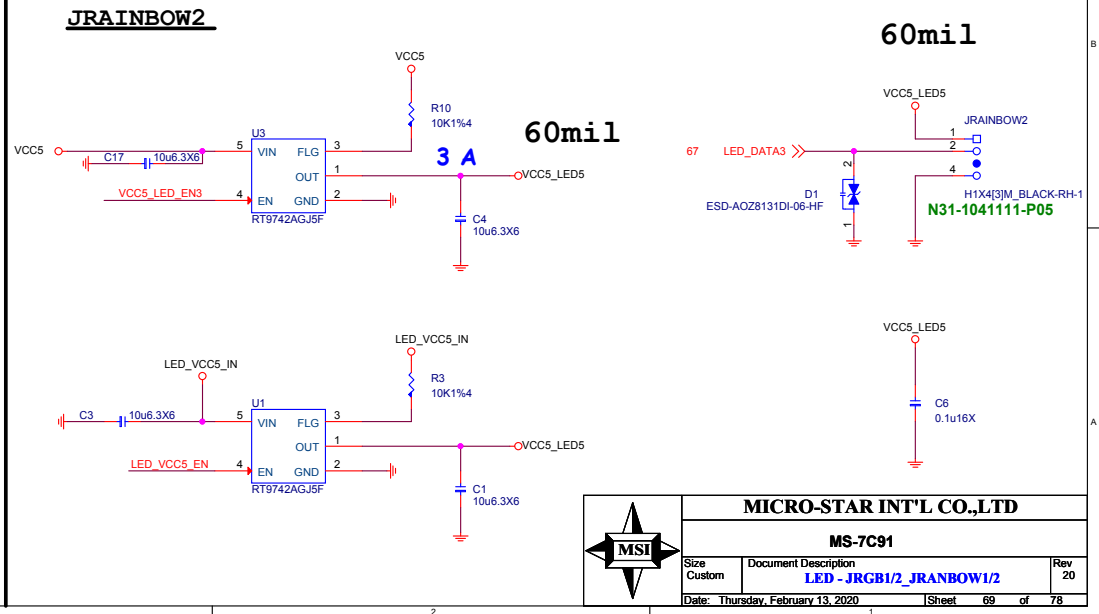


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JRGB1

JRGB2JRAINBOW1JRAINBOW2

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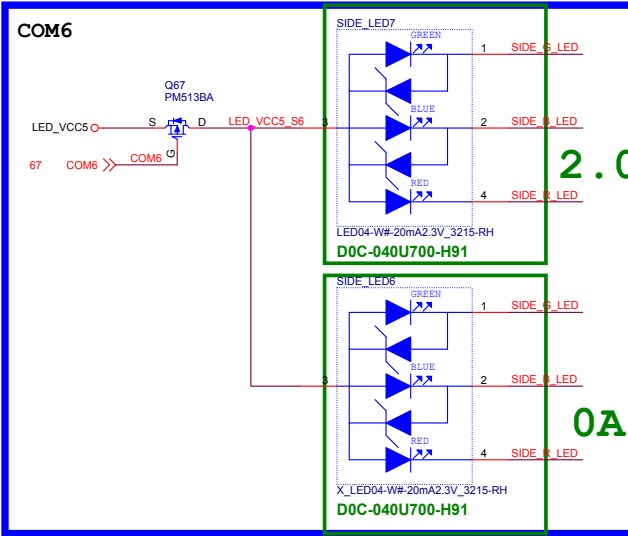
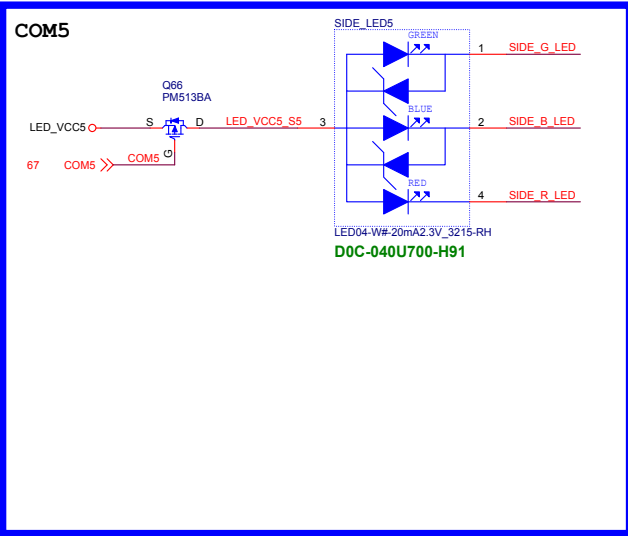
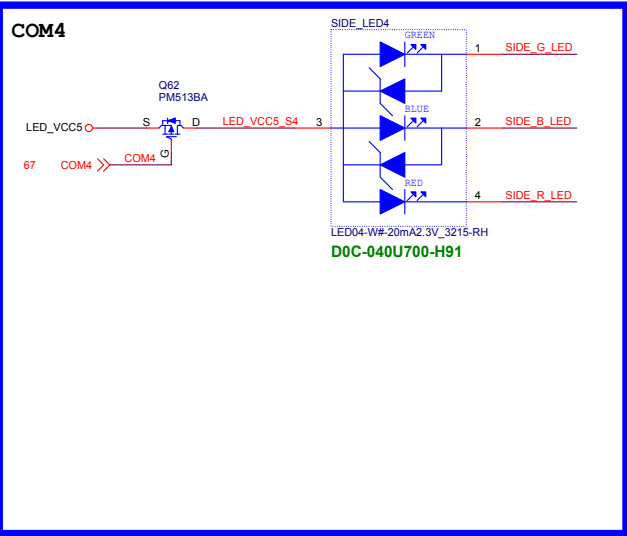
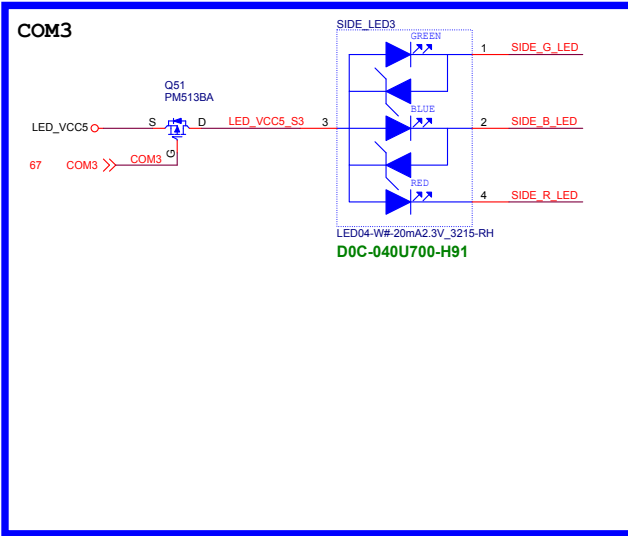
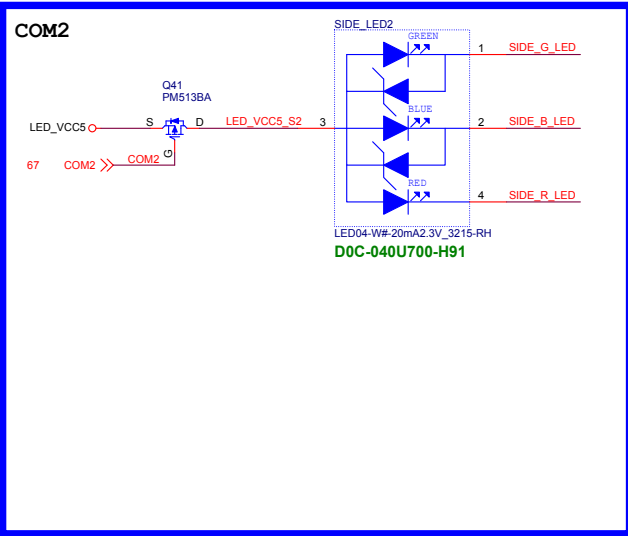
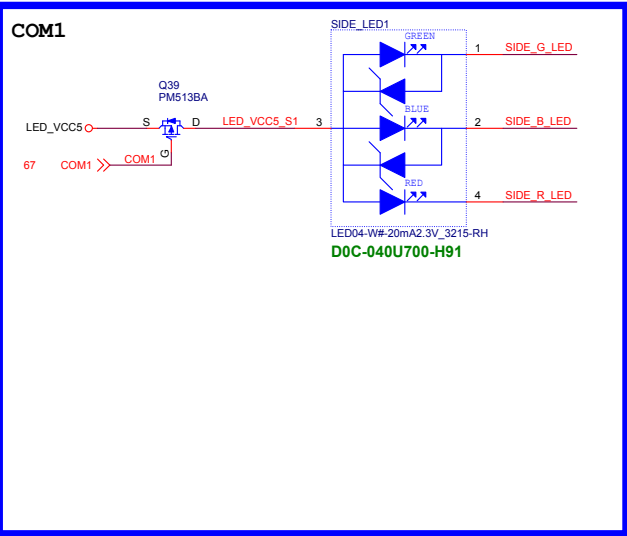
MS-7C91

Size	Document Description
Custom	<b>LED - JRGB1/2_JRANBOW1/2</b>

Rev

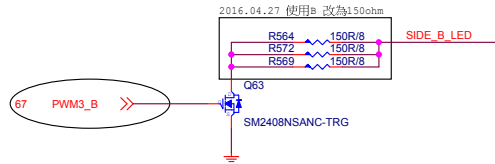
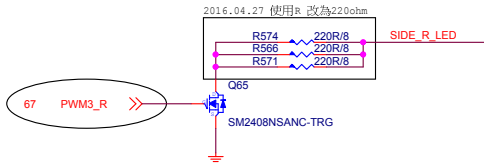
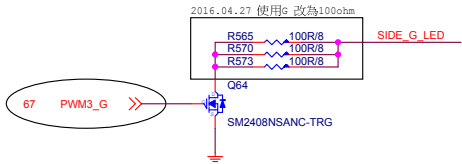
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BOARD SIDE LED \*6



2.0 BOM

0A BOM



5	4	3	2	1
D				D
C				C
B				B
A				A



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CPU Socket



E95-0000022-A91

PCB

PCB1



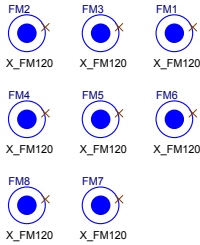
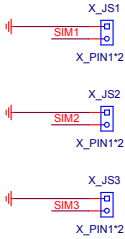
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PD0-07C9120-G37

MOS HEATSINK

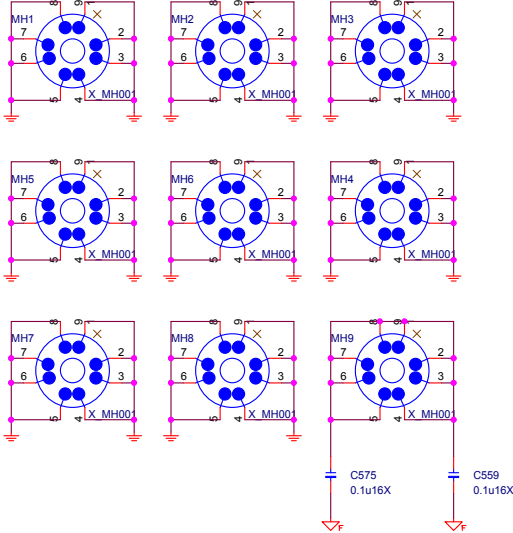
N MOS      W MOS

IO COVER

Simulation



Optics Orientation Holes



MANUAL PART

AMI\_LAB1  
G51-M1SPXXA-A09  
G51-M1SPXXA-A09

CFOS1  
Y02-MU00170-CFO  
Y02-MU00170-CFO

HDMI\_LA1  
Label  
HDMI  
HDMI LABEL  
Y01-RHDMI03-000

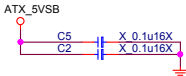
MKT\_LA1  
Label  
MKT LABEL  
X\_MKT LABEL  
G51-M1SPP78-Q13

BAT1\_XT  
BAT-BCR2032P

AV1:  
D06-0100161-P52  
D06-0100101-R26

Moat CAP

Reserve for bypass 12VIN noise use



PCH HEATSINK

Audio COVER

DDR COVER

20190201 Remove DDR\_COVER1